Processor and field-programmable gate arrays (FPGAs) perform the heavy lifting in most embedded systems. While processors and FPGAs often work alone, the two technologies work brilliantly together, forming an even more powerful embedded computing platform. Often in these systems, the processor provides the high-level management functionality while the FPGA performs stringent real-time operations, extreme data processing, or interface functions not easily supported by a processor.

SoC FPGA devices successfully integrate both processor and FPGA architectures in a single device. Melding the two technologies provides a variety of benefits including higher integration, lower power, smaller board size and higher bandwidth communication between the processor and FPGA. Best-in-class devices exploit the unique advantages of a merged processor/FPGA system while retaining the benefits of stand-alone processor and FPGA.

An SoC FPGA provides at least comparable and likely superior functionality and performance than previous generation designs, but at a lower board space, lower power and lower system cost—maybe as much as 50% less. By integrating these technologies on the same piece of silicon, system developers can eliminate the cost of one of the plastic packages. If both the CPU and FPGA in a design use separate external memories, designers may also be able to consolidate both into one memory device, saving even more system cost, board space and power. Because the signals between the processor and the FPGA now reside on the same silicon, communication between the two consumes substantially less power compared to using separate chips. Plus, thanks to thousands of internal connections between the processor and the FPGA, an integrated solution has substantially higher bandwidth and lower latency compared to a two-chip solution.

There are several design considerations and engineering decisions embedded developers should take into account when choosing the best SoC FPGA for their application. These selection criteria include system performance, system reliability, power consumption, development tools and future roadmap.

Increasing System Performance with SoC FPGAs

Ultimately, system performance in SoC FPGAs is dictated by efficiently moving data between four major SoC functions: the processor, the FPGA logic, the interconnect, and on-chip and off-chip memory.

In a variety of applications, system performance is dominated by the data path performance, where a device must process continuous streams of data at “line speed” or “wire speed” with a minimum of stalling or interruptions. In these applications, the FPGA logic crunches the critical data path while the processor provides high-level management over the control path. The processor intercepts a small fraction of the incoming data and mostly attempts to stay out of the way of the data path.

To perform this delicate dance, modern-day SoC FPGAs leverage an ARM dual-core Cortex-A9 application...
processor integrated into the fabric of an advanced 28nm FPGA. The Cortex-A9 offers an ideal mixture of low power, capabilities, bandwidth and performance compared to other application processors.

The interconnect featured in Cyclone V SoCs is designed specifically to increase system performance by supporting more than 100 Gbit/s of throughput between the FPGA logic and the processor (Figure 1). The 100 Gbit/s interconnect between the FPGA logic and the Cortex-A9 processor ensures the system has sufficient interconnect performance to support high-throughput traffic.

The ability to efficiently access on-chip and off-chip memory also enables SoC FPGAs to increase system performance. Hardened memory controllers featured in Cyclone V SoCs employ advanced algorithms to squeeze as much memory efficiency as possible. These algorithms extract maximum bandwidth by managing transaction priority, reordering command and data, and scheduling pending transactions using algorithms like deficit weighted round robin. Additional performance comes by customizing the memory controller via software to best fit a custom data profile.

When evaluating the performance of a memory controller, it is important to not just look at the bus width and speed. System level benchmarks, such as LMbench, are useful for assessing the overall performance of the memory subsystem. As evidenced by running the LMbench benchmark on a 667 MHz Cyclone V SoC system, the Cyclone V SoC with the smarter memory controller extracts more memory bandwidth—up to 17% more than a competitive SoC device—despite a 25% lower memory operating frequency. This efficiency advantage enables the Cyclone V SoC to deliver more bandwidth at lower clock rates, resulting in system power savings.

Increasing System Reliability with SoC FPGAs

As memory sizes continue to increase, the need for error detection and correction is a growing trend in designs today. Most modern systems include dedicated hardware to help ensure data integrity. This includes error correction code (ECC) protection—not only as part of the memory controller, but also integrated within the processor’s on-chip memories, caches, peripheral buffers and in the FPGA itself. Error checking and correction circuitry makes a system more robust and resilient against unexpected data errors or corrupted data.

Memory protection is a feature often associated with the memory controllers in more advanced processors, whether called a memory management unit (MMU) or memory protection unit (MPU). The processor’s memory protection unit prevents errant or illegal processor transactions from reading or corrupting other memory regions. In the Cortex-A9 processor, ARM extends this protection concept with TrustZone, which provides a system-wide approach for security-sensitive systems.

Using the Cyclone V SoC, specific memory regions may be dedicated to the operating system and embedded software applications while other memory regions may be dedicated to FPGA-based functions, as shown in Figure 2. Via memory protection, the FPGA master functions are prevented from corrupting the operating system or embedded software regions.

Integration Leads to Power Savings

New electronics applications are increasingly power aware—and not just in handheld devices, but also in automotive applications and even server racks with their seemingly endless power and cooling budget. SoC FPGA devices are viable solutions to help embedded developers stay within their power budgets.

As illustrated in Figure 3, simply integrating the processor and FPGA components into a single SoC FPGA can potentially reduce system power by 10% to 30%. I/Os carrying signals between devices, often at higher voltages, are one of the most power-consuming functions in an application.

Beyond the power savings that simple integration provides, Cyclone V SoCs feature power-saving modes such as clock gating and scaling. The processor and FPGA also have independent power planes, allowing an application to turn off power to the FPGA completely while keeping the processor active to monitor any interrupts.

To optimize power, SoC designs are becoming more interrelated with power supply design. At a system level, the power supply design often consumes more power than the SoC device itself. The challenge in these systems is bal-
sis tools. Software ultimately determines bugging, software debugging and analysis in the FPGA tools, on-chip and more energy-efficient electronic hardware must be matched by similar innovation in the FPGA tools. However, the innovation in and more energy-efficient electronic products. However, the innovation in and more energy-efficient electronic hardware must be matched by similar innovation in the FPGA tools. However, the innovation in and more energy-efficient electronic hardware must be matched by similar innovation in the FPGA tools. However, the innovation in and more energy-efficient electronic hardware must be matched by similar innovation in the FPGA tools. However, the innovation in and more energy-efficient electronic hardware must be matched by similar innovation in the FPGA tools. However, the innovation in and more energy-efficient electronic hardware must be matched by similar innovation in the FPGA tools. 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set of peripherals, on-chip memory, a high-speed internal interconnect architecture, a hierarchy of on-chip memory and a leading-edge FPGA fabric. Innovative new software design and debug tools enable developers to simultaneously view and cross-trigger both sides (processor and FPGA) of the chip. While the available devices on the market may seem similar at first glance, upon a closer look, the underlying architecture matters.

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**FIGURE 4**
Stratix 10 SoCs are the third-generation SoC from Altera, which integrates a quad-core Cortex-A53 processor built on Intel’s 14 nm Tri-Gate process technology.

**Altera Announces Quad-Core 64-bit ARM Cortex-A53 for Stratix 10 SoCs**

Altera’s Stratix 10 SoC devices, manufactured on Intel’s 14nm Tri-Gate process, will now incorporate a high-performance, quad-core 64-bit ARM Cortex-A53 processor system, complementing the device’s floating-point digital signal processing (DSP) blocks and high-performance FPGA fabric. Coupled with Altera’s system-level design tools, including OpenCL, this versatile heterogeneous computing platform will offer exceptional adaptability, performance, power efficiency and design productivity for a broad range of applications, including data center computing acceleration, radar systems and communications infrastructure.

The ARM Cortex-A53 processor, the first 64-bit processor used on an SoC FPGA, is an attractive fit for use in Stratix 10 SoCs due to its performance, power efficiency, data throughput and advanced features. The Cortex-A53 is among the most power-efficient of ARM’s application-class processors, and when delivered on the 14nm Tri-Gate process will achieve over six times more data throughput compared to today’s highest performing SoC FPGAs. The Cortex-A53 also delivers important features, such as virtualization support, 256 Tbyte memory reach and error correction code (ECC) on L1 and L2 caches. Furthermore, the Cortex-A53 core can run in 32-bit mode, which will run Cortex-A9 operating systems and code unmodified, allowing a smooth upgrade path from Altera’s 28nm and 20nm SoC FPGAs. Leveraging Intel’s 14nm Tri-Gate process and an enhanced high-performance architecture, Altera Stratix 10 SoCs will have a programmable-logic performance level of more than 1 GHz—two times the core performance of current high-end 28nm FPGAs.

By standardizing on ARM processors across its three-generation SoC portfolio, Altera will offer software compatibility and a common ARM ecosystem of tools and operating system support. Embedded developers will be able to accelerate debug cycles with Altera’s SoC Embedded Design Suite (EDS) featuring the ARM Development Studio 5 (DS-5) Altera Edition toolkit, the industry’s only FPGA-adaptive debug tool, as well as use Altera’s software development kit (SDK) for OpenCL to create heterogeneous implementations using the OpenCL high-level design language. Stratix 10 SoCs will offer designers a versatile and powerful heterogeneous compute platform enabling them to innovate and get to market faster.