APPLICATION NOTE

I^2C Communication for VPX55-3 Power Supply

Communicating through I2C with an NAI VPX55-3 Power Supply

Description

I^2C is a bi-directional, two wire serial bus which provides communication using a data line and clock line (SDA and SCL).

Using I^2C Communication on NAI, VPX55-3 Power Supplies

1. Hardware Interface.

   Electrical interface is based on I2C parameters at 100 kHz. The backplane or I2C master controller should provide pull up resistors on SDA (Data) and SCL (Clock) lines to a 3.3V rail. On the NAI **VPX55-3,** the SDA line is located on Pin D5 (SM0) and the SCL line is located on pin C5 (SM1).

2. Address.

   The I2C Address is 7 bits. Default base address is 0x20. *GA0, and *GA1 provides 2 LSB's for the address. The *GA pins have pull-up resistors internal to the power supply to 3.3V. When left open, the address will be 0x20, with both grounded the address will be 0x23, see table below.

Pin		I2C Address
*GA1	*GA0	
Pin B5	Pin A5	
High	High	0x20
High	Gnd	0x21
Gnd	High	0x22
Gnd	Gnd	0x23

3. Data Read.
   No command is necessary. Perform an I2C read of 1 to 58 Bytes of 8 Bit Data. It is not required to read the entire data string. An I2C start condition will reset the read sequence to byte zero (0).

BYTE #	Data Type	Meaning
0	Status Register 0, MS Bit First	Refer to table below
1	Status Register 1, MS Bit First	Refer to table below
2-3	U Integer, MSB First	Temperature as follows °C = (Reading * 0.6445) -280
4-5	U Integer, MSB First	Voltage on VS3, 5V = 16384
6-7	U Integer, MSB First	Voltage on VS2, 3.3V = 16384
8-9	U Integer, MSB First	Voltage on VS1, 12V = 16384
10-11	U Integer, MSB First	Voltage on 3.3Aux, 3.3V = 16384
12-13	U Integer, MSB First	Current on VS3, 40A = 16384
14-15	U Integer, MSB First	Current on VS2, 20A = 16384
16-17	U Integer, MSB First	Current on VS1, 15A = 16384
18-19	U Integer, MSB First	Current on 3.3Aux, 4A = 16384
20-37	Reserved	
38-51	Character String	Part Number
54-55	U Integer	S/N Hi
56-57	U Integer	S/N Low

Status Reg 0								
bit	7	6	5	4	3	2	1	0
	x	x	x	x	x	x	-12AuxGood	+12AuxGood

Bits 0 and 1 (+12AuxGood, -12AuxGood) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.

Status Reg 1								
bit	7	6	5	4	3	2	1	0
	x	FAIL	OTWarning	SWPriority	*SW Inh	*SW En	*HW Inh	*HW En

Bits 5 AND 6 (OTWarning - FAIL) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.

Bit 4 (SWPriority) is Read and write. It is clear at Startup. When clear the unit will be controlled by the hardware enable and inhibit signals. When set, the unit will be controlled by the SW inhibit and enable signals.
Bits 3 and 2 (SWInh SWEn) are read and write. Their logic works the same as the logic for the hardware Enable and Inhibit.

*SWEnable	*SWInhibit	OUTPUTS
0	0	INHIBIT (3.3V Aux is On, all other outputs are off)
0	1	ON
1	0	OFF
1	1	OFF

Bits 1 and 0 (HWIn - HWEn) are read only. They show the state of *Enable and *Inhibit pins while SWPriority is low.

4. Status Write Command

The command to write to Status bytes 'zero and one' is 55h, followed by 8-bit data for byte zero and 8-bit data for byte one. For error detection purposes, bytes zero and one have to be sent twice for the command to take effect.

Example to Send a command to clear the faults and turn on all the outputs, the following sequence must be sent.

55h 03h 78h 03h 78h;

55h is the command needed to write to bytes zero and one.
03h data for byte zero, where bits 0 & 1 are being set.
78h data for byte one,

Bit 7 set: don't care bit.
bit 6 set: FAIL signal is high, software will clear it if unit fails
bit 5 set: OTWarning signal is high, software will clear it if unit is close to 75 degrees.
bit 4 set: Software has priority to enable/disable unit.
bit 3 set: SWInhibit is high
bit 2 low: SWEnable is low.

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