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APPLICATION NOTE

LVDT Four Wire Mode Setup Procedure

Purpose:

The purpose of this document is to provide the necessary steps to configure an LVDT module that measures the position of an LVDT transducer in four wire mode configuration.

Assumption:

- Excitation Voltage = 3Vrms
- Excitation Frequency = 400Hz
- Channel one is used in the LVDT module.
- Use auto bandwidth in the LVDT module.
- Default Ch1 Bandwidth = 40Hz
- Use 4-wire configuration in the LVDT module
- Power already applied to the LVDT module.

Overview:

In general, the following steps are needed to configure the LVDT module:

1. Wire-up a LVDT transducer to one of the channels (Ch.1 for this app. note) to the LVDT module as shown in Fig1.
2. Apply excitation (Ref) voltage to the transducer.
3. Setup up Ch1 Signal Loss Threshold.
4. Setup up Ch1 REF Loss Threshold.
5. Setup up Bandwidth Select.
6. Setup up Ch1 Bandwidth.
7. Setup LVDT2W/LVDT4W mode.
8. Setup LVDT1 Scale.
9. Setup LD Active Channels.
10. Setup Test Enable.
11. Check no BIT Status (CH1-4) for Ch1.
12. Check no SIG Status (CH1-4) for Ch1.
13. Check no REF Status (CH1-4) for Ch1.
14. Loop steps 11 to 13 at least two times with 200ms delay apart. If failures persisted from step 14, check wiring connection.
15. Read Position CH1 Data Lo then Position CH1 Data Hi register and determine current LVDT position.

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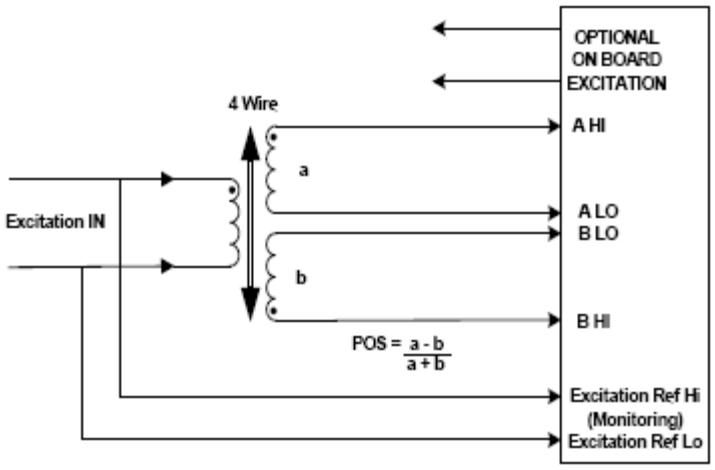

Fig1. LVDT Configuration: 4-Wire Mode

Steps In Detail:

1. Wire-up the LVDT module as shown in Fig1.
   1-a. Setup excitation voltage to 3Vrms and frequency to 400Hz.

2. Apply excitation(Ref) voltage to the transducer.
   2-a. Connect LVDT transducer to the LVDT module channel 1 as shown in Fig1.

3. Setup up Ch1 signal loss threshold
   3-a. Set signal loss threshold to 90% of maximum input voltage of the transducer. So signal loss threshold = 3* 0.9 = 2.7V.
   3-b. Covert 2.7V to the register value of signal loss threshold. So 2.7/0.01=270(0x10E).
   3-c. Write 0x10E to the signal loss threshold register for Ch1.

4. Setup up Ch1 Ref loss threshold
   4-a. Set Ref loss threshold to 90% of maximum input voltage of the transducer. So Ref loss threshold = 3 * 0.9 = 2.7V.
   4-b. Covert 2.7V to the register value of Ref loss threshold. So 2.7/0.01=270(0x10E).
   4-c. Write 0x10E to the Ref loss threshold register for Ch1.

5. Setup up Bandwidth select
   5-a. This register is bitmapped per channel; (i.e. D0=Ch1, D1=Ch2, etc). "1" indicates user wants automatic bandwidth. "0" is in manual bandwidth.
   Write 0x1 to Bandwidth select register to set channel one to be in auto bandwidth.

6. Setup up Ch1 Bandwidth
   6-a. In order for the auto bandwidth to work, write 0x2A and then 0x28 to Ch1 Bandwidth register. So write 0x2A and then 0x28 to the Ch1 Bandwidth register.

7. Setup LVDT2W/LVDT4W mode
   7-a. This register is bitmapped per channel; (i.e. D0D1=Ch1, D2D3=Ch2, etc). "1" indicates user wants 4-wire. "2" is in 2-wire mode.
   Write 0x55 to LVDT2W/LVDT4W mode register to ALL channels to 4-wire mode.

8. Setup LVDT1 scale
   8-a. This register increase resolution but reduces the observing displacement in the LVDT system. For instance, if a LVDT transducer has a linear stoke range of +/- 4 inches and the LVDT1 scale is set to 0xFFFF which is the default value, at + 4 inches the LVDT Ch1 will read 49.9985 and that is the maximum position full scale from LVDT module. To improve resolution for a particular interested range; said +/- 2 inches, you would have to change the LVDT1 scale by a half to 0x7FFF. Therefore, at the position of +2 inches the LVDT1 ch1 will read 49.9985 and that is the maximum position full scale range of the LVDT module on channel one.
   8-b. Write the value 0xFFFF to the LVDT1 scale for normal resolution. See Table 1 for the effect of LVDT scaling.

9. Setup LD Active Channels
   9-a. This register is bitmapped per channel; (i.e. D0=Ch1, D1=Ch2, etc). "1" indicates active channels. "0" is not in active channel. Write 0x1 to LD Active Channels register to set channel one to active.

10. Setup Test Enable
    10-a. This register is bitmapped for different Test mode; (i.e. 0x1=D0 Test, 0x4=D2 Test, and 0x8=D3 Test). Write 0x4 to the Test Enable register to enable D2 test for the LVDT board.

11. Check no BIT Status on Ch1.
    11-a. This register is bitmapped per channel; (i.e. D0=Ch1, D1=Ch2, etc). "1" indicates a BIT failure. "0" indicates no BIT failures. Read the BIT Status register a few times and make sure no BIT failure is reported.

12. Check no SIG Status on Ch1.
    12-a. This register is bitmapped per channel; (i.e. D0=Ch1, D1=Ch2, etc). "1" indicates a SIG failure. "0" indicates no SIG failures. Read the SIG Status register a few times and make sure no SIG failure is reported.

13. Check no REF Status on Ch1.
    13-a. This register is bitmapped per channel; (i.e. D0=Ch1, D1=Ch2, etc). "1" indicates a REF failure. "0" indicates no REF failures. Read the REF Status register a few times and make sure no REF failure is reported.

14. Loop steps 11 to 13 at least two times with time delay of 200ms apart. If failures persisted from step 14, check wiring connections.

15. No status failures. Read Position registers and determines current LVDT position for channel 1.
    15-a. Read the Position Ch1 Data Lo Register and then read the Position Ch1 Data Hi Register. Make sure read the Lo register first. To get the position, concatenate the Position Ch1 Data Lo to Position Ch1 Data Hi to form a 32 bit signed integer value. The actual position is calculated by using the concatenated position value times 50 and divided by 2147483647 (i.e. 0x7FFFFFFF).

Item	Ahi-Alo (Vrms)	Bhi-Blo (Vrms)	LVDT Scale	Pos. Ch1 Hi	Pos. Ch1 Lo	Position (%) +50%=Positive Full Scale	Comments
1	2.1170	2.1175	0xFFFF	0x2	0x2400	0	Normal scale.
2	2.3639	1.8389	0xFFFF	0x1000	0xAC00	6.2492	Normal scale.
3	2.5681	1.5413	0xFFFF	0x2000	0xC000	12.5013	Normal scale.
4	2.7248	1.2406	0xFFFF	0x3000	0xD400	18.745	Normal scale.
5	2.8408	0.9475	0xFFFF	0x4000	0x4400	25.0004	Normal scale.
6	2.9944	0.02	0xFFFF	0x7FFF	0x0000	49.9985	Normal scale.
7	2.1170	2.1175	0x7FFF	0x2	0x1C00	0	Scale reduced by half.
8	2.3639	1.8389	0x7FFF	0x2000	0xB000	12.5012	Scale reduced by half.
9	2.5681	1.5413	0x7FFF	0x4000	0x9000	25.0004	Scale reduced by half.
10	2.7248	1.2406	0x7FFF	0x5FFA	0x3400	37.5100	Scale reduced by half.
11	2.8408	0.9475	0x7FFF	0x7FFF	0x0000	49.9985	Scale reduced by half.
12	2.9944	0.02	0x7FFF	0x7FFF	0x0000	49.9985	Beyond monitored range. Ch. saturated

Table 1: Effects of LVDT Scaling

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