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Intelligent I/O Approach Lets Developers Right-Size Systems

Sometimes an SBC-centric design means unnecessary overhead. An intelligent I/O strategy shortens SBC selection process and reduces obsolescence risk.

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It's a fact that today's demanding military embedded systems require lots of processing horsepower to perform a plethora of mission-critical applications. Much attention is given to the processor or SBC selection. Systems integrators are spending countless days, weeks and even months comparing, contrasting and evaluating SBC boards from COTS vendors that most closely meet their overall system needs before making a final decision. Inevitably, the time spent in this "discovery" phase of a program tends to push the deadline further and further to the right.

Commercial off-the-shelf vendors offer a multitude of SBC boards that meet today's challenging processing requirements for military embedded systems customers. They range from 3U and 6U cPCI, 6U VME, and 3U and 6U OpenVPX, taking advantage of both Intel and Freescale processor offerings. ARM processors are also starting to catch the eye of system integrators, noting the processing performance and the lower power required. COTS SBC boards typically support the same basic core processing function coupled with onboard I/O and a mezzanine site. The core processing function offers the basics: processor, SDRAM, boot and user flash, serial ports, Ethernet ports, some general purpose I/O (GPIO) ports and options for USB, Video or SATA interfaces.

Predetermined I/O on SBCs

All those interfaces are predetermined on the SBC board and vary from vendor to vendor. In addition, no two vendors support the same I/O routing to the user-defined pins for any of these standard I/O interfaces. Each one defines the onboard rear I/O routing based on the history of board designs. In order to support additional I/O requirements, COTS vendors add mezzanine card sites to their SBC offering. These cards are known as PCI Mezzanine Cards (PMC), or Switched Mezzanine Cards (XMC). In most cases they require one or more PCIe to PCI Bridge chips to interface to the PMC. PCIe can be routed directly to XMC sites. They can range in functionality from simple discrete I/O to the most complex high-speed A/D with DSP and FPGA processing.

In recent years some COTS vendors have started adding non-standard mezzanine sites to their 6U VME and OpenVPX SBC boards, which continue to utilize the PCI bus interface. These non-standard mezzanine sites enable vendors to offer the most commonly used military embedded I/O interfaces without compromising the use of the PMC or XMC site(s). Common interfaces on these non-standard sites include MIL-STD-1553, video, flash storage and SCSI. They can also be used to fulfill a standard I/O requirement that eliminates the need for additional PMC/XMC carrier cards. Therefore, a 6U VME or 6U OpenVPX card could typically support up to three additional I/O and communications functions using a PMC, XMC or non-standard mezzanine site.

Carrier Card Approach

Carrier cards are used to add I/O support in systems without having to use another SBC. Therefore, one SBC is managing all of its onboard I/O, its PMC/XMC I/O and any other I/O found on separate PMC or XMC carrier cards that contain PMC, XMC or non-standard mezzanine cards. In 6U VME or cPCI this is usually done by routing a PCI bus on the backplane from the SBC to the carrier card(s); or in 6U OpenVPX, a PCIe or multiple PCIe interfaces are routed on the backplane from the SBC to the carrier card. A PCIe switch is located on the carrier card to route PCIe to XMC cards or to PCIe-to-PCI interface chip(s) for connectivity to PMC cards.

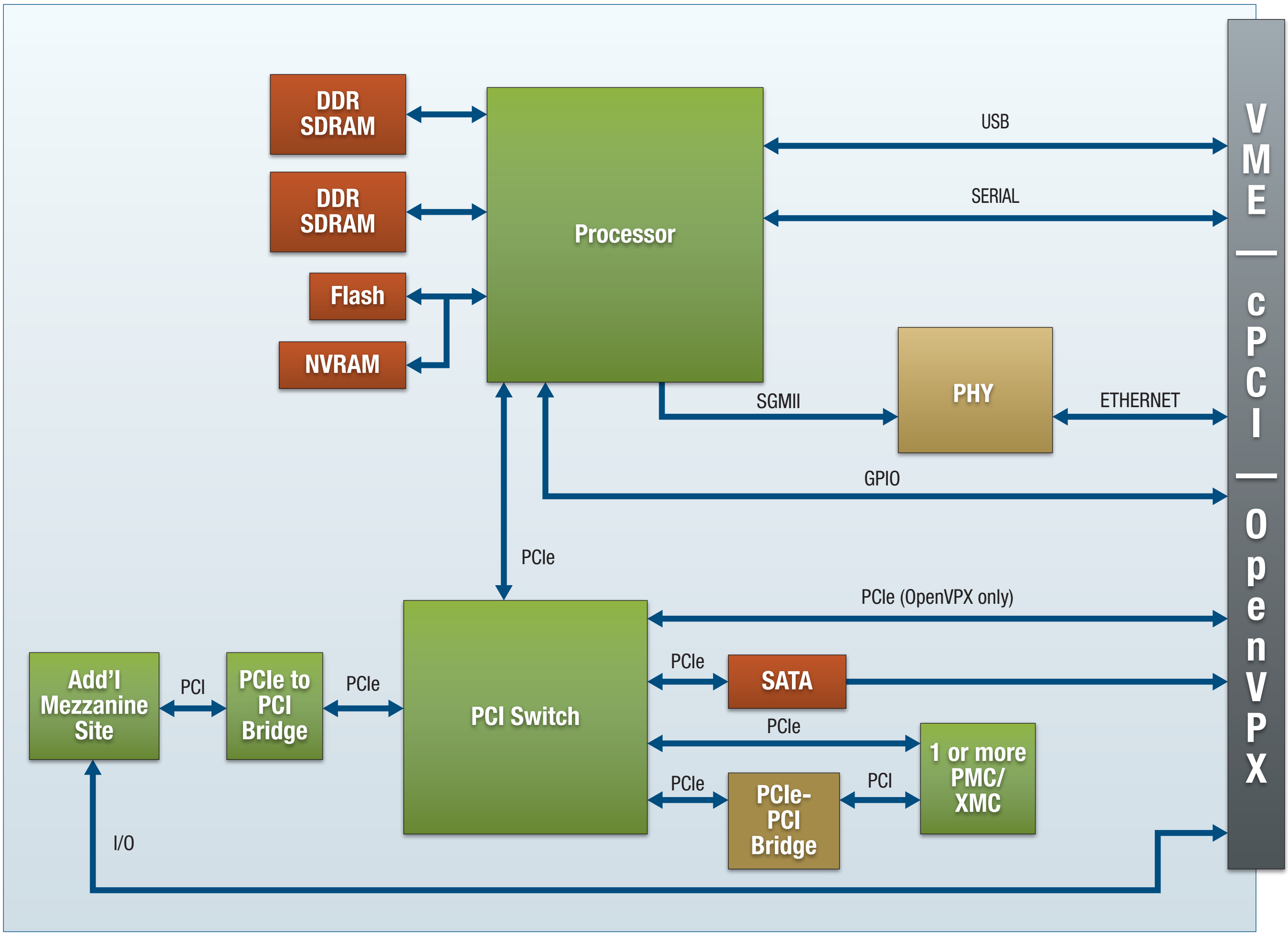

Figure 1

Diagram of a typical COTS SBC with PMC/XMC sites.

A military embedded system containing an SBC with PMC, XMC, another mezzanine site and PMC/XMC carrier cards is an example of just one of the ways in which systems integrators can meet their processing and I/O requirements (Figure 1). More and more hardware engineers are desperately seeking ways to eliminate the need to use an SBC with fixed I/O and communications, not to mention the restrictions inherent in 6U VME/VPX of up to three additional I/O or communications functions. In 3U the limit is either one I/O or communication function. The ability to select an SBC and also select the I/O and communications functions is an engineer's preferred approach—for instance, not just one to three of them but more in the area of at least two functions for 3U and up to six functions in 6U.

Software Overhead Implications

As described above, most of the I/O interfaces require drivers specifically written for the processor type—Intel, Freescale and so on—and a Real Time OS. Imagine a small system that monitors 32 to 48 discretes, 20 to 30 200 KHz A/D and D/A signals; supports three or four CANBus interfaces, three or four RS-232/422/423/485 channels, dual-channel dual-redundant MIL-STD-1553 interfaces; and simulates or measures five to six Synchro-Resolver interfaces. This system typically requires two, three or more 6U VME or OpenVPX boards—more boards would be needed if it were 3U cPCI or 3U OpenVPX. The SBC could support the serial ports on board; MIL-STD-1553 would be supported via a non-standard mezzanine site on the SBC; Discretes and A/D could be PMC/XMCs on the SBC; and the rest could be supported via the use of carrier cards. All of these communications and I/O functions are usually handled by the only intelligent chip in the system: the SBC processor.

Besides executing the embedded application—also known in this case as the Operational Flight Program (OFP)—, the SBC has to manage and control all of the I/O interfaces. Built-in Test (BIT), a must in military embedded systems, is also handled by the SBC processor. In addition, military embedded systems sometimes require the SBC processor to have anywhere from 25 to 50 percent of spare processing overhead. Unfortunately, when you add up all of the processing required by the SBC to support the I/O, BIT and spare overhead, it leaves little processing resource for the application. Now imagine a system that has many more I/O and communications functions, which in turn increases BIT processing. As you add I/O functionality you eat away at processing available for use by the application or for spare processing overhead. Ideally, a solution using Intelligent I/O would relieve the SBC of the handling of all the processing associated with the I/O functions.

Protecting Software Investment

Often the drivers for I/O functions and application software take many man-months to write and lots of money to support and validate. Unfortunately, we are all well aware of the dreaded obsolescence notification. Systems integrators are concerned about potential end-of-life components. The sheer thought of components going end-of-life sends shivers up the spines of systems integrators and program mangers of military embedded defense and aerospace programs all over the world. Think about how the software engineers feel. They have to write a new driver for the replacement chip, integrate a new Board Support Package (BSP) from the SBC vendor for the OS and update the application code. Not to mention all of the regression testing that needs to be performed.

Consider the advantages if all the software that supports the I/O functions were 100% protected from obsolescence. Ideally, all I/O would be handled by a library call to read/write from/to an I/O function in a fixed memory space that doesn't change. Additional I/O memory space can be added for enhancements but the previous I/O memory mapped space remains intact. All the I/O memory mapped function data could be made available on the system interfaces like VME, cPCI, PCIe, sRIO or even Ethernet. The application software and in turn the software engineer would never have to

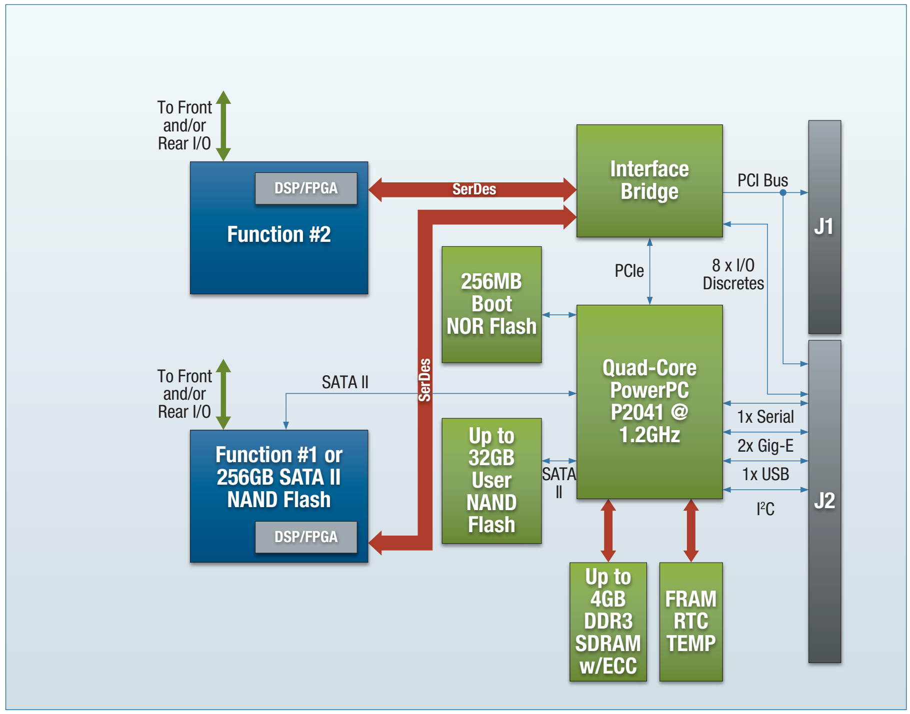

Figure 2

Diagram of a NAI 75SBC4 with two function slots.

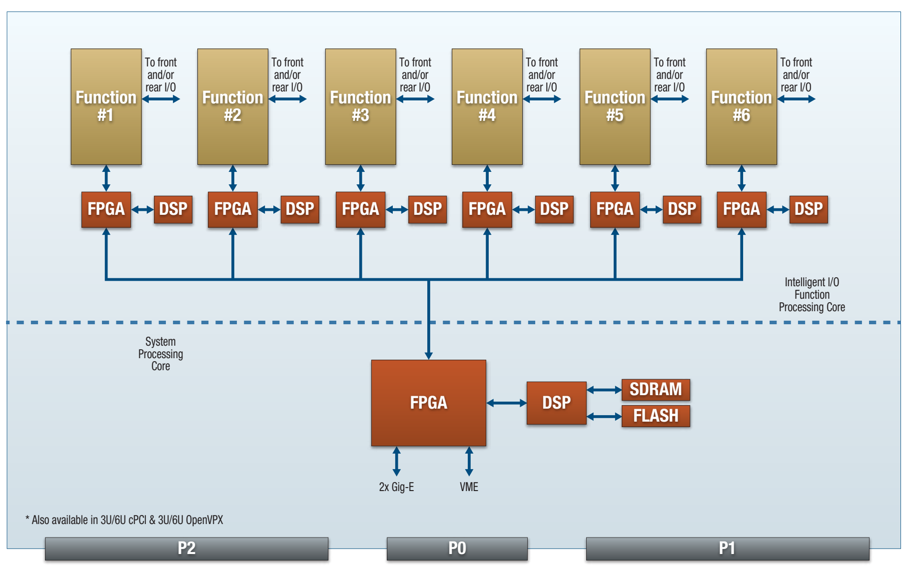

Figure 3

This intelligent I/O approach supports the protocol overhead and programmable configuration of the I/O functions, BIT for each of the I/O functions, and maintains a VME, cPCI, PCIe, sRIO or Ethernet interface.

deal with an I/O driver running on the SBC (Figure 2).

If the I/O function hardware goes obsolete, a new one that exists in the same exact memory space containing the same exact configuration registers would replace it, making it completely invisible to the application running on the SBC. In

Figure 4

The SIU6 is a subsystem that manages and controls up to 12 different I/O functions without the need of an SBC.

addition, if the I/O functions had intelligence to function on their own and also execute continuous BIT, it would isolate the SBC from having to process I/O functionality and BIT. This would in essence reduce the risk of obsolescence for the overall system and also relieve processing overhead from the SBC processor.

Intelligent I/O without an SBC

Does every military embedded subsystem require an SBC? Perhaps not, but systems integrators have become so accustomed to assigning a VME, cPCI or OpenVPX slot to an SBC of some kind that it has become second nature. In reality, if the subsystems connected to the main mission computers were able to manage and control all I/O functions, there would be no need for an SBC in these subsystems. The key is to add the I/O intelligence to the subsystem handling the I/O function without the need for an SBC. In most cases the SBC in the mission computer is handling lots of I/O overhead including multiple serial protocols, A/D and D/A conversion, status of multiple discretes and anything that is connected to it on the PCI/PCIe bus from PMC or XMC cards.

If the mission computer's only responsibility was to execute the application while all of the data it needed was given to it when available or when the mission computer had data to send, it would alleviate processing resources for the SBC in the mission computer. Some COTS vendors have implemented intelligent I/O PMC/XMC cards but they still require an SBC or carrier card to be mounted on, and in most cases the carrier cards cannot interface with other boards in the system.

An intelligent I/O solution (Figure 3) would support: the protocol overhead and programmable configuration of the I/O functions, BIT for each of the I/O functions, and maintain a VME, cPCI, PCIe, sRIO or Ethernet interface. The solution would be flexible enough to be configured with a host of I/O functions to support a large percentage of subsystem requirements for today's demanding military embedded systems. It would have to be low power and support high density I/O.

Advantage of Eliminating SBC

North Atlantic Industries' Intelligent I/O architecture, coupled with its complete line of power supply offerings, takes it one step further when installed in an SIU6 (Figure 4), a subsystem that manages and controls up to 12 different I/O functions without the need of an SBC. All data is sent to or read from the SIU6 by the mission computer over an Ethernet interface. All protocol and BIT processing overhead is handled by the Intelligent I/O functions within the SIU6. The SIU6 comes configured with five MIL-STD-38999 connectors, three 100-pin connectors for I/O, one rugged Quadrax connector for Dual Gigabit Ethernet Interfaces and one power input connector. The chassis and backplane with connectors is built and sold the same way every time. The only options are the power input requirements and the I/O functions defined by the customer. Future I/O functions can be added, removed, or changed without any impact to backplane wiring. This saves a lot of development time and non-recurring engineering costs. The best part is eliminating the need for a potentially power hungry SBC.

Now more than ever systems integrators demand intelligent high-density, low-power, flexible I/O. Budgets are tight and modified COTS I/O products requiring any NRE dollars are not the systems integrator's logical choice. They want field-proven, mix-and-match I/O that meets the requirements of the product specification. For systems integrators, offloading any processing overhead is a plus and can make the difference in winning a major program.

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