# Special Feature

Multifunction I/O Boards

# Distributed Strategies Tame Complex Sensor/Control I/O Demands

Faced with the onslaught of ever greater compute density and I/O density requirements, strategies like distributed processing and distributed I/O architectures are becoming more and more attractive.

Paul Feldman, V.P. of Digital Design Engineering
North Atlantic Industries

Modern military platforms continue to place an ever greater reliance on electronics for their operation. Just as aircraft have transitioned to fly-by-wire systems, ground vehicles are transitioning to drive-by-wire. At the same time, greater numbers of sensors are being incorporated into sea, air and ground vehicles. These are used to detect everything from incoming projectiles to engine vibration. Moreover, an increasing number of electronically controlled actuators are being used to affect a response based on the sensor data. Each of these sensors and actuators must be connected to some type of I/O point to collect data for processing. As an example, consider a simple turn-by-wire design. The operator (driver) turns right, requiring an input measurement. Then a control point is used to activate the correct actuator to change wheel position around the vertical axis.

Figure 1

Submarines are particularly heavy users of sensors. A significant number of vibration sensors are needed on a modern submarine to ensure complete stealth. Shown here, the Virginia-class fast attack submarine USS Virginia (SSN 774) cruises through the Bay of Naples.

All this raises a number of questions. How do we fit this increased electronic content, interconnect all of these sensors without increasing weight, and finally process this exponential increase in data? If the electronics are replacing a mechanical system—like a mechanical steering system—the added electronics are usually lighter and smaller than the system being replaced, albeit at the cost of higher processing requirements. Many times, however, sensors are added to increase performance, without an associated decrease in space and weight. As always, more electronics implies higher processing requirements and an increased number of interconnects.

## Multifunction I/O Strategies

To accommodate this increased level of electronics, manufacturers are implementing a number of strategies. First, by using high levels of integration, a far larger number of I/O points can be placed on a single PCB today than in the recent past. Although certainly not proceeding at the same pace as digital electronics integration, none the less, analog integration is proceeding along a rapid slope. Where five years ago, 32 A/D convertors or D/A convertors on a single PCB was considered high density, today 60 or more is commonplace. In fact, it is now to the point that the number of analog functions that can be placed on a PCB is limited more by the number of I/O pins on the connectors than on the density of the electronics that can fit in a given PCB real estate.

To address this problem, manufacturers are turning to VPX from VME or cPCI. VPX has approximately twice the I/O of VME. Second, the I/O boards being provided today are "smart." These boards not only perform A/D, D/A or simple I/O functions, they also provide sophisticated levels of data processing. For example, simple I/O boards have A/D converters that sample the input data at some rate, and send that data to a mission computer for processing. Modern military ships, submarines, aircraft and even ground vehicles can have many thousands of points to sample. For example, think of the number of vibration sensors needed on a modern submarine to ensure complete stealth (Figure 1).

Meanwhile, in an effort to gain more information over ever increasing bandwidths, the sampling rate is increasing from a few thousand Hz to over 100 KHz, with bit depths increasing from 12 bits to 16 and 24. These data rates can easily overwhelm the most powerful processor, especially when complex algorithms like FFTs and FIR filtering need to be performed. With onboard FPGAs and DSPs as shown in Figure 2, the I/O board manufacturer can easily provide pre-processing to offload the main processor. Since these components are highly programmable, the hardware of these COTS boards remains the same, but the functions provided are highly configurable, either by the I/O board provider, or the end-user systems integrator.

## Minimizing SWaP

These "smart" boards provide another very important feature that minimizes system size and power (SWaP); the ability to perform multiple functions on one PCB. In the past, many boards were available with 32 or 64 A/Ds or D/As, or 28V discretes, as well as separate boards for different types of communication functions (MIL-STD-1553, serial, ARINC429, CANBus, etc.) and processing (SBCs). Many systems, however, require smaller numbers of many different types of I/O and communications. To address this, manufacturers have created multifunction VME, cPCI and VPX boards. These boards allow the system integrator to select from a large number of available functions, and incorporate smaller channel counts of many functions on one PCB.

This is made possible through the ability of the base board FPGAs and DSPs to be programmed at final assembly to perform almost any task. For example, a single board can incorporate A/D, D/A, RTD, MIL-STD-1553, ARINC429 and 28V discretes, just to name a few (dozens of different functions are available). Another possibility is a multifunction I/O board that contains SBC (either PowerPC or Intel) support, along with the ability to provide large combinations of the many available functions. This single board can replace up to six dedicated boards. Just as importantly, these multifunction boards are COTS. The base board and the modules are designed, tested and stocked by the manufacturer. The system integrator simply orders the board with the required functions. The manufacturer performs the final assembly, downloads the necessary FPGA/DSP code and performs final test.

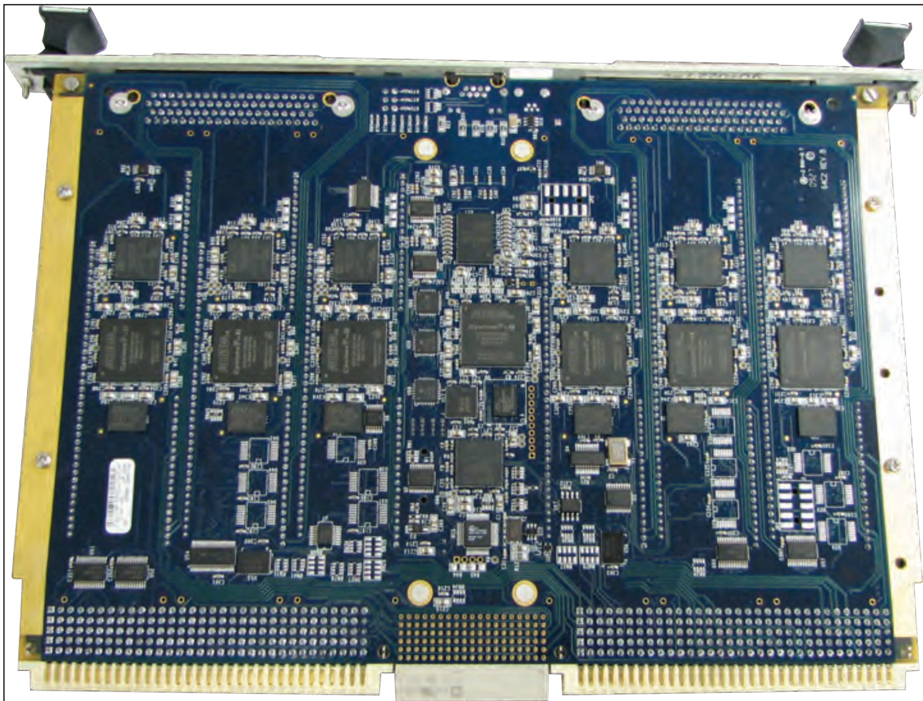

Figure 2

Onboard FPGAs and DSPs as shown here enable I/O board manufacturers to provide pre-processing to offload a system's main processor. This allows the functions provided to be highly configurable, either by the I/O board provider or the end-user systems integrator.

## Moving to Distributed I/O

The next level up is a strategy that is just starting to take shape; distributing I/O data and processing. This concept is extremely powerful, and can simultaneously solve a host of issues. The I/O chassis Sensor Interface Unit (SIU) is usually some type of rugged self-contained design, which includes the necessary power supply, configurable I/O, communications with the mission processor and an optional SBC function. This approach allows system integrators to place I/O points very near the actual sensors, pre-process the data, and then send the reduced data back to the mission proces-

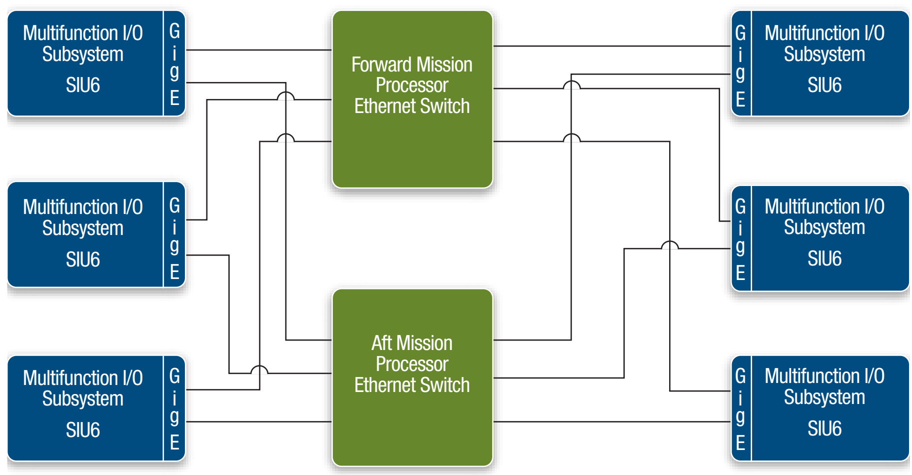


Figure 3

In this conceptual redundant system design, each SIU has two or more Gbit Ethernet or other communications channels, so each is always connected to both the main and redundant mission computers. The main mission computer can stay in control of the system, despite various hardware failures.

sor. For example, going back to the simple turn-by-wire design, the system requires an input function that can measure the position of the steering wheel (A/D, S/D or Encoder), measure the position of the drive wheel around the vertical axis (another A/D, S/D or Encoder), and a D/A or PWM to actually drive an actuator to turn the wheel.

The main processor would most likely need to implement a control loop to perform this function. In addition, a number of cables now need to run from the sensors and actuators back to the main processor chassis, which also houses the I/O functions. Now imagine a remote self-contained SIU or multiple SIUs depending on the size of the platform, which contains all of the I/O functions needed to perform this task, as well as an SBC function. The SIU can be placed close to the sensors and actuators to implement the control loop necessary to perform the actual function. In this scenario, the main processor doesn't need to implement a control loop, but would simply read the steering wheel position and only have to send a short message to the remote SIU that said, as an example, "turn 6 degrees," significantly reducing the main processing load.

Another major advantage is reduction in cable length. This reduction has the advantage of not only a potentially significant reduction in weight, but also in reduced noise pickup, wire losses, ground loop potentials, and in many cases significantly reduced EMI. This can be most advantageous in aircraft, where hundreds of wires now need to travel only a few feet, versus 100 feet or more, or in ships and submarines, which can be many hundreds of feet in length. The weight difference between 100 twisted/shielded pairs, 50 feet in length vs. a dual Gbit Ethernet wire or fiber connection of the same length is enormous, greater than a 10-1 reduction. Since the SIU uses standard 28 VDC or single/three-phase 115 VAC, the power cabling to the SIU is also short, as this standard power is usually available across the entire platform at many points.

## Maintenance and Redundancy

Maintenance is also reduced and made easier by the fact that these SIUs are usually intelligent and incorporate extensive BIT, making them self-diagnosing. If an SIU fails, it is much simpler for maintenance personnel to isolate the problem and replace a chassis with four or five connectors than it is to try to diagnose a problem with a system that contains tens of boards, find the bad board and replace it, usually taking down an entire rack of equipment in the process. Reduced cabling also helps in maintenance and system availability. Instead of running hundreds of signals hundreds or even thousands of feet, we can now run just a few fiber optic cables, each of which can contain redundant fibers. If one of the fiber connections fails, a technician can easily isolate the bad fiber and switch to a redundant one.

Redundancy is another area where this approach excels. In the past, redundant systems required entire racks of equipment to be duplicated, with the issue of who decides which rack is in control, along with which processor. Usually, if anything failed in one rack, the entire rack needed to be shut down, and the backup took over. With distributed SIUs, the task not only becomes easier to manage, it also has an inherent "fail-soft" property. Since each SIU controls a subset of all platform functions, if an SIU fails, only that subset needs to be switched over to the backup hardware. Additionally, each SIU has two or more Gbit Ethernet or other communications channels, so each is always connected to both the main and redundant mission computers. The main mission computer can stay in control of the system, despite various hardware failures. Figure 3 shows a conceptual redundant system design using this approach.

## Combining 1553, ARINC 429 and More

As an example, North Atlantic Industries offers a "standard" SIU that supports up to 300 I/O points, configurable for many different I/O functions, supports the equivalent of an SBC to process data, and communicates to the main mission processor over a multitude of communication interfaces including GigE, MIL-STD-1553, ARINC429 and CANBus, just to name a few. This SIU is shown in Figure 4. One of the main advantages of this SIU is that it is a fully qualified COTS design that can be configured to meet the system integrator's needs, yet be delivered quickly with little or no NRE.

As with both consumer and industrial systems, the trend toward greater electronic content in military platforms will accelerate, due to the many advantages that smart electronics provides. Although increased use of electronics can provide significant advantages to the modern system designer, its application must be approached carefully. With the ever increasing number of I/O points, along with higher sampling rates, greater dynamic range and greater functionality implemented using electronic I/O, a system can quickly become difficult to implement and maintain. Clearly, using both intelligent I/O boards and distributed I/O SIUs not only reduces the processing requirements of the main system processors and significantly reduce cable weight, it also provides for a simpler system implementation that is more easily maintained. This will push the electronic content of present and future military platforms ever higher.

North Atlantic Industries
Bohemia, NY.
(631) 567-1100.
[www.naii.com].


Figure 4

Box-level SIUs like this can support up to 300 I/O points, configurable for many different I/O functions, supports the equivalent of an SBC to process data, and communicates to the main mission processor over a multitude of communication interfaces including Gbit Ethernet, MIL-STD-1553, ARINC429 and CANBus.