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POWER SUPPLY APPLICATION NOTE



VPX56-6 Series I²C Communication Guide

Overview

I²C Communication is standard on all NAI VPX power Supplies. I²C is used for both monitoring and control of many power supply functions including output health, temperature and ENABLE* / INHIBIT* Control.

I²C Communication on the VPX56-6 Series

Hardware Interface

Electrical interface is based on I²C parameters at 100 kHz. The backplane or I²C master controller should provide pull up resistors on SDA and SCL lines to a 3.3V rail.

Address

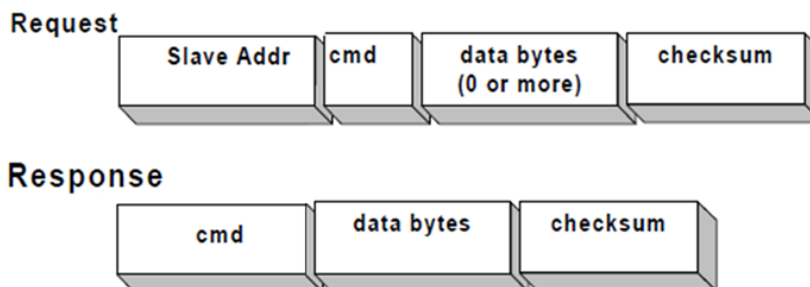
The I²C Hardware Address (per VITA 46.11 Rev 0.15) is 7 bits. The default base address is 0x20. *GA0 through *GA4 provide the 5 LSB's for the address.

The *GA pins have 3.32K pull-up resistors to a 3.3V rail. The resistors and the 3.3V rail are internal to the power supply. When left open, the address will be 0x20, otherwise, the address will be as described in the table below.

Signal						I ² C Address
*GAP	*GA4	*GA3	*GA2	*GA1	*GA0	
Pin A5	Pin B5	Pin A4	Pin B4	Pin C4	Pin D4	
Gnd	High	High	High	High	High	0x20
High	High	High	High	High	Gnd	0x21
High	High	High	High	Gnd	High	0x22
Gnd	High	High	High	Gnd	Gnd	0x23
High	High	High	Gnd	High	High	0x24
Gnd	High	High	Gnd	High	Gnd	0x25
Gnd	High	High	Gnd	Gnd	High	0x26
High	High	High	Gnd	Gnd	Gnd	0x27

If the unit detects an error on the *GAP input setting, it will respond to address 0x20.

Data Read - Get Sensor Reading results



	Byte	Data Field	Data
Request Data	1	cmd	See table
	2 to n-1	Data If Required by cmd or Zero ChkSum* if no Data required.	
	n	Zero ChkSum* if Data was required by cmd	
Response Data	1	Completion Code – Echo cmd Number	
	2 to n-1	Per cmd Response	
	n	Zero ChkSum	

*Note : Slave address should not be included in Zero Checksum calculation.

Commands

Sensor #	Name	Description
21H	Composite Sensor	64 bytes of scanned sensor data. Data is continually scanned and available for report. Data consists of 2 bytes of data for each of the 11 sensors and FRU data.
55H	Status Write Command	Writes Status byte on Composite Sensor.
44H	Firmware release date	22 byte response. Month/Day/Year Hr/Min/Sec in ASCII form.
45H	Hardware Address	3 byte response. Reports address set by GA0*-GA4*

Composite Sensor Read Command – 21H

Response BYTE #	Data Type	Meaning
0	Completion Code – 21h	Echo of the command
1	Status Register 0, MS Bit First	Refer to table below
2-3	Signed Integer, MSB First	Temperature as follows °C = (Reading * 100 / 16384)
4-5	U Integer, MSB First	Voltage on VS1, 12V = 16384
6-7		Reserved
8-9	U Integer, MSB First	Voltage on VS3, 5V = 16384
10-11	U Integer, MSB First	Voltage on 3.3Aux, 3.3V = 16384
12-13	U Integer, MSB First	Voltage on +12V Aux, 12V = 16384
14-15	U Integer, MSB First	Absolute Voltage on -12V Aux, 12V = 16384
16-17	U Integer, MSB First	Current on VS1, 30A = 16384
18-19		Reserved
20-21	U Integer, MSB First	Current on VS3, 50A = 16384
22-23	U Integer, MSB First	Current on 3.3Aux, 20A = 16384
24-25	U Integer, MSB First	Current on +12VAux, 3A = 16384
26-27	U Integer, MSB First	Absolute Current on -12VAux, 3A = 16384
28-29	U Integer, MSB First	Internal Reference, 2.5V = 16384
30-31		Reserved
32-51	Character String	Part Number
52-53	U Integer, MSB First	S/N Hi
54-55	U Integer, MSB First	S/N Low
56-57	U Integer, MSB First	Date Code (Year/Week)
58-59	U Integer, MSB First	Hardware Rev
60-61	U Integer, MSB First	Firmware Rev.
62	Reserved	Reserved
63	Zero Checksum	Value required to make the sum of bytes 0 to 62 add to a multiple of 256 (decimal).

Status Reg 0		R/Set	R/Set	R/W	R/W	R/W	R	R
Bit	7	6	5	4	3	2	1	0
	x	FAIL	OTWarning	SWPriority	*SW Inh	*SW En	*HW Inh	*HW En

Bits 5 AND 6 (OTWarning - FAIL) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.

Bit 4 (SWPriority) is Read and write. It is clear at Startup. When clear the unit will be controlled by the hardware enable and inhibit signals. When set, the unit will be controlled by the SW inhibit and enable signals.

Bits 3 and 2 (*SWInh *SWEn) are read and write. Their logic works the same as the logic for the hardware Enable and Inhibit.

*SWEnable	*SWInhibit	OUTPUTS
0	0	INHIBIT (3.3V Aux is On, all other outputs are off)
0	1	ON
1	0	OFF
1	1	OFF

Bits 1 and 0 (HWIn - HWEn) are read only. They show the state of *Enable and *Inhibit pins while SWPriority is low.

Status Write Command - 55H

BYTE #	Data Type	Meaning
0	U Character – 55H	Command
1	U Character	Data
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

The command to write to Status byte is 55h, followed by 8-bit data then zero checksum.

Example: To send a command to clear the faults and turn on all the outputs, the following sequence must be sent.

55h 78h 33h;

55h is the command needed to write to status byte zero.

78h data for byte zero,

Bit 7 set: don't care bit.

Bit 6 set: FAIL signal is high, software will clear it if unit fails

Bit 5 set: OTWarning signal is high, software will clear it if unit is close to 75 degrees.

Bit 4 set: Software has priority to enable/disable unit.

bit 3 set: SWInhibit is high

bit 2 low: SWEnable is low.

33h Value to achieve a sum of zero.

Firmware release date – 44H

Response BYTE #	Data Type	Meaning
0	Completion Code – 44H	Echo of the command
1-20	Character String	Date
21	Zero Checksum	Value required to make the sum of bytes 0 to 20 add to a multiple of 256 (decimal).

Hardware Address – 45H

Response BYTE #	Data Type	Meaning
0	Completion Code – 45H	Echo of the command
1	U Character	I ² C Hardware Address
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

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