Scope

The intent of this application note is to provide a guide to the understanding and maximum utilization of NAI 2nd generation Digital to Synchro – Resolver (D/S-R) converter modules. The terminology 2nd generation" is used to distinguish the current converter design characteristics from NAI's initial designs which are still popular, in production and in wide spread use.

The new designs are the result of a "technology insertion" to the initial design architecture. Both designs use Digital Signal Processors (DSP's), Field Programmable Gate Arrays (FPGA's) and sophisticated software algorithms, along with conventional electronic components, to implement the converter functions.

The availability of much higher speed DSP's and larger FPGA's integrated on each module as opposed to earlier designs which shared less capable devices across multiple modules, has enabled the creation of converters featuring unprecedented flexibility, programming options and enhanced performance. Many of the new features are also a result of years of experience and feedback from our customer base.

Added Features / Programming options

The 2nd generation converters have many added features and programming options as follows;

- Auto Ranging 2-115 V rms reference voltage input
- Synthesized reference, eliminates noise and harmonics
- Measured Output V L-L
- Measured Reference Voltage and Frequency
- Choice of Fixed or Ratiometric output mode
- Programmable Output V L-L
- Higher power outputs (1.5 / 2.2 or 3 VA)
- Torque Receiver (TR) Mode (Single channel units only)
- Programmable Reference to Output Turns Ratio (Ratiometric Mode)
- Dedicated Wrap S/D for each D/S-R Channel
- Programmable Loss of Signal (LOS) threshold
- Programmable Loss of Reference (LOR) threshold
- Choice of External analog or Programmable trigger for Rotation mode start
- Phase Lock Loss status
- Programmable phase shift

Table of Contents

Introduction

This User Guide is structured for ease of use and in such a way as to serve both experienced and novice users of Synchro / Resolver Simulation devices (D/S & D/R converters). Toward that end, the following Sections and Reference information (Appendices) are provided.

- Section I - Beyond just generating Synchro / Resolver signals.
  - Functional block diagram / Description - New 2nd generation converters.
  - Added features.
- Section II Modules and Platforms applicability.
- Section III Quick Start Guide – "I know about S/R simulation, lets generate some angles!"
  - Analog I/O connections to Synchros & Resolvers
  - Minimum required initial programming
- Section IV - BIT / Diagnostics / D3 detail setup

Reference Material

- Appendix A – Detailed Module specs.
- Appendix B – Pin outs / I/O Signal definitions
- Appendix C – VME and PCI / cPCI Memory maps
- Appendix D – Transducers
  - Transducers, Synchros and Resolvers
  - Simplified, basic D/S-R converter theory
- Appendix E - Glossary of terms and abbreviations

Section I – Detail Description 2nd Generation Converters

General

The last page of this section is a functional block diagram (BD) depicting the functions & features of the new converters. Keep in mind that the functional blocks shown and described are implemented via a High speed DSP processor in conjunction with an FPGA, running sophisticated digital algorithms, along with electronic components, to perform the various block functions shown. The blocks are not depictions of actual electronic components.

(Note: The BD, if viewed on your computer screen, is best if magnified to 120 %)

User Digital Interface

Referring to the BD, the information (functions) shown going to and from the block(s) titled "DSP & FPGA Logic and Registers" are the various user programming commands and "read" data available through the digital interface bus (PCI, cPCI, or VME). The titles correlate to the sections / descriptions found in the detail Operations Manual for the particular Platform in use under the heading "D/S ONE/TWO CHANNEL (MODULE ##*). They are also consistent with the Register Memory maps provided in the manuals and included as "Appendix C" in this document.

User Analog Interface

Shown on the right side of the BD is the analog signal interface for the converter channel. In the most basic interface situation, only the Synchro / Resolver Outputs and the reference input will be available. Sense line connections will be internally installed at the time of board configuration. (e.g.- See Appendix B – Pin outs / I/O Signal definitions for the 76CS3).

Where pin out availability is sufficient, Sense lines are brought to this connector to allow optional remote load sensing. Tying the Sense lines at the load is only necessary in rare applications where the converter is supplying full power (1.5, 2.2 or 3 VA) and the distance to the load is significant such that the potential exists for unacceptable V L-L reduction. Keep in mind that Synchro / Resolver interfaces are capable of operating accurately with L-L voltage drops of as much as 20% or more. Therefore, connecting the sense lines at the load will most likely be unnecessary in most applications. Where remote load sensing is not needed and the sense lines are available, they should be looped back at the analog interface connector. **(THE SENSE LINES MUST BE CONNECTED!)**

Other possible signals which may be available are the optional connections to an auxiliary Synchro Booster Amplifier (SBA) such as the NAI 44PA1. Interfacing to an SBA can be as simple as connecting the Synchro or Resolver signals to the input of the SBA. However, again where available, additional control and error monitoring connections to the SBA are possible. A separate application note will detail both simple and more complicated interfacing with the 44PA1 SBA.

The last Analog interface connection is an External "Rotation Start" input. At this time, this optional control is only implemented on the certain platforms. This is a differential input (Trig + and Trig -). For Rotation mode start control, the user must select either a digitally programmed Start command or the external Analog input. If the Analog input is selected then triggering on the rising or falling edge of the trigger signal can also be controlled via the digital interface.

Reference Processing & Monitoring

An area of the new design which was improved significantly is the processing of the reference signal input.

Features include;

- Auto ranging 2-115 V rms reference voltage input – no need to provide an exact voltage level to guarantee a specific output L-L Voltage unless output mode is set to Ratiometric.
- Measured Reference Voltage & Frequency – User can read the actual measured reference input voltage and frequency.
- Synthesized reference eliminates noise and harmonics. This reference is then used in the generation of the D/R Sine and Cosine outputs and used for the Wrap S/D Converter reference input.
- Programmable Loss of Reference (LOR) threshold level, allowing the user to define the level at which LOR status is flagged.

D/R Converter / Digital Angle Processing

Ironically, the D/R function is probably the simplest function implemented. Digital Sine and Cosine of the programmed D/S Write Angle are used to generate analog outputs. As with the simple D/R covered in Section 1, the Sine and Cosine signals are the result of multiplying the synthesized analog reference input by the digital Sine and Cosine of the commanded angle.

The digital Sine and Cosine are supplied by the Digital Angle Processing function based on the commanded position (D/S Write Angle). Other functions requiring Digital commanded angles to the D/R include;

- Test angle generator – generates 24 digital test angles for the D3 Offline test.

- Rotation control – monitors and controls all aspects of the Rotation functions. Including, rotation rate / direction, rotation mode (Start / Stop or Continuous), and rotation start (whether by digital command or by analog input).

- Two speed angle generation – Each two channel D/S module (1* & 2* series) can be used as a Two speed pair, generating 1x & Nx analog outputs on channel one and two. When in two speed,(D/S 2 speed Ratio Mode), channel one outputs the Course angle (1x) for the two speed set. The processor multiplies the 1x programmed D/S Write Angle by the programmed speed ratio (N) and outputs a D/S Write Angle for the second channel which is serving as the Fine channel (Nx). Thus, in two speed mode, the user only needs to command the 1x angle.

- Torque Receiver routine – Applies only to the single channel modules (3* & 4*). This feature allows these 3 VA output converters to drive small / medium sized TR's without the need for an External booster amplifier.

  TR loads have a large dynamic range of drive VA requirements. A TR is an "active" load and it generates Synchro stator signals just like a TX, CX or D/S that's commanding it to a position. When a transmitters' output angle is the same as the Rotor position of a TR, very little current is required to hold that position. There is very little transfer of power as the two sets of Stator signals are for the most part equal. Likewise, moving a TR to a new position, if commanded in small steps, is also a low power demand condition. Only when the commanded angle is first applied to a TR whose Rotor position is significantly different, will there be a high power demand on the D/S. This condition will also occur for large programmed angle steps.

How the TR routine works

If the load demand exceeds the 3 VA capability of the single channel modules, then the module will sense an over current condition and internally disconnect the D/S outputs from the TR. This will also trigger the TR software / hardware routine. However, the TR is still connected to the Analog interface connector and now appears like a transmitter and these signals are being presented to the Wrap S/D converter. The wrap S/D reads the TR position and that angle is sent to the D/S as a new commanded angle. The D/S output is enabled and reconnected to the TR but the two devices are now synchronized and VA required is minimal.

The routine then calculates the difference between the originally commanded D/S angle and sends a series of small step angles to the D/S to rotate the TR to the initial desired angle.

Thereafter, the user should take steps to program changes in commanded position in small increments. How big a step which can be commanded without triggering another TR Routine may have to be determined by experiment.

Wrap S/D Converter / Output Level Monitor & Control

The Wrap S/D (WSD) converters' primary function is to monitor the D/S-R converter analog output angle to implement the continuous on-line BIT feature (D2 Test). The digital output of this converter is continuously compared to the commanded D/S Write Angle. If the angles are not within 0.2 degrees, a BIT Status flag will be set indicating a failure and the Red front panel BIT LED will be turned on**. Note, a complete loss of the reference signal or the output signal will also activate the Red BIT light since it will cause an accuracy (D2) test failure.** While LOR and LOS thresholds can be set to any value, LOS and LOR flags will not necessarily cause a D2 failure. It is suggested that the user read the Operations Manual descriptions for these functions. Also see Section IV of this application note for more details on the BIT functions.

In addition to measuring the output Angle position information, this function block compares the output angle signal amplitude with the user programmed LOS Threshold to flag an LOS Status and also provides the user with the output signal measured amplitude (Measured Signal Voltage).

As shown in the block diagram, the inputs to the WSD are the Sense lines. Where not available at the Analog I/O connector the Sense lines are routed to the WSD input via internal jumpers. If available on the Analog I/O connector being used, these **Sense signals must be connected for proper operation**.

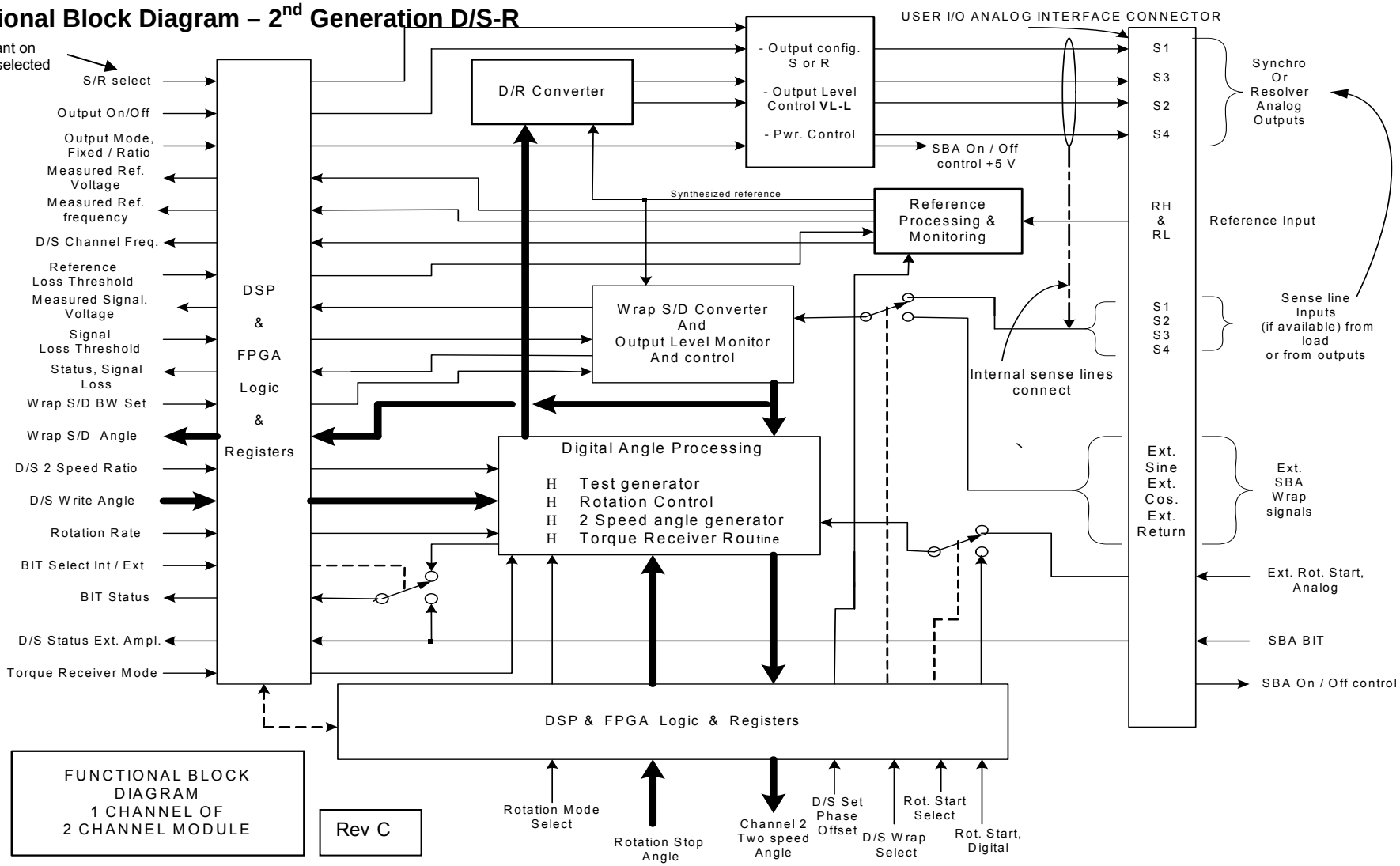
Alternatively, the input to the WSD can be Ext Sine & Ext Cosine feedback from an external SBA (NAI model 44PA1) allowing the WSD to compare the SBA output signals to the commanded angle which provides a more complete system BIT test.

Output configuration, level & power control.

The outputs of the D/R converter are the analog Sine and Cosine signals and they are operated on in the block shown for configuring the final output signals as either Resolver format or Synchro format. The signals are presented to Buffer amplifiers which are just two amplifiers for Resolver configuration outputs or amplifiers setup to provide a Scott T function which will generate 3 wire Synchro configuration output signals. This output block also sets the desired output V L-L voltage programmed by the user. This output block also provides solid state switching (ON / OFF) of the amplifier outputs.

The balance of functions depicted in the BD are self explanatory.

Functional Block Diagram – 2nd Generation D/S-R



Section II – Applicable Modules and Platforms

Note the following module code tables are shown here for reference only. Additional modules will be added and these tables will not necessarily reflect the updated lists. For the up to date module listings, please refer to the "Operations Manuals" posted on our web site for each Platform.

Dual Channel D/S-R Module Code Table (1*& 2*)

Code	Format	Output (V_{L-L}) (Vrms)	Ref (V_{REF}) (Vrms)	Frequency (Hz)	Max Load (VA)
10	SYN	2 – 28	2 – 115	360 – 1.1K	1.5
11	RSL	2 – 28	2 – 115	360 – 1.1K	1.5
12*	PRG S / R	2 – 28	2 – 115	360 – 1.1K	1.5
13	SYN / RSL	2 – 28	2 – 115	360 – 1.1K	1.5
14	RSL / SYN	2 – 28	2 – 115	360 – 1.1K	1.5
15	SYN	2 – 28	2 – 115	47 - 440	1.5
16	RSL	2 – 28	2 – 115	47 - 440	1.5
17*	PRG S / R	2 – 28	2 – 115	47 - 440	1.5
18	SYN / RSL	2 – 28	2 – 115	47 - 440	1.5
19	RSL / SYN	2 – 28	2 – 115	47 - 440	1.5
1A	RSL	2 – 28	2 – 115	1K – 3K	1.5
1B	RSL	2 – 28	2 – 115	3K – 5K	1.5
1C	RSL	2 – 28	2 – 115	5K – 7K	1.5
1D	RSL	2 – 28	2 – 115	7K – 10K	1.5
1E	SYN	2 - 11.8	2 – 115	400 – 1K	1.5
1F	SYN	2 - 11.8	2 – 115	47 – 400	1.5
1G	SYN	2 - 11.8	2 – 115	1K – 3K	1.5
1H	SYN	2 - 11.8	2 – 115	3K – 5K	1.5
1J	SYN	2 - 11.8	2 – 115	5K – 7K	1.5
1K	SYN	2 - 11.8	2 – 115	7K – 10K	1.5
1L	SYN	2 – 28	2 – 115	1K – 3K	1.5
1M	SYN	2 – 28	2 – 115	3K – 5K	1.5
1N	SYN	2 – 28	2 – 115	5K – 7K	1.5
1P	SYN	2 – 28	2 – 115	7K – 10K	1.5
20	SYN	90	2 – 115	360 – 1.1K	2.2
21	RSL	90	2 – 115	360 – 1.1K	2.2
22*	PRG S / R	90	2 – 115	360 – 1.1K	2.2
23	SYN / RSL	90	2 – 115	360 – 1.1K	2.2
24	RSL / SYN	90	2 – 115	360 – 1.1K	2.2
25	SYN	90	2 – 115	47 - 440	2.2
26	RSL	90	2 – 115	47 - 440	2.2
27*	PRG S / R	90	2 – 115	47 - 440	2.2
28	SYN / RSL	90	2 – 115	47 - 440	2.2
29	RSL / SYN	90	2 – 115	47 - 440	2.2

*Note: Synchro or Resolver programmability uses a miniature mechanical relay for this task. This capability is not recommended for Military embedded applications.
** There is a +10% tolerance on the upper limit, -0% on the lower limit (i.e. 115V +10%, 126V Max)

Single Channel D/S-R Module Code Table (3* & 4*)

Code	Format	Output (V_{L-L}) (Vrms)	Ref (V_{REF})** (Vrms)	Frequency (Hz)	Max Load (VA)
30	SYN	11.8	2 – 115	400 – 1K	3.0
31	RSL	2 – 28	2 – 115	400 – 1K	3.0
35	SYN	11.8	2 – 115	47 - 440	3.0
36	RSL	2 – 28	2 – 115	47 - 440	3.0
3A	RSL	2 – 28	2 – 115	1K – 3K	3.0
3B	RSL	2 – 28	2 – 115	3K – 5K	3.0
3C	RSL	2 – 28	2 – 115	5K – 7K	3.0
3D	RSL	2 – 28	2 – 115	7K – 10K	3.0
3E	SYN	2 - 11.8	2 – 115	1K – 3K	3.0
3F	SYN	2 - 11.8	2 – 115	3K – 5K	3.0
3G	SYN	2 - 11.8	2 – 115	5K – 7K	3.0
3H	SYN	2 - 11.8	2 – 115	7K – 10K	3.0
3J	SYN	2 – 28	2 – 115	1K – 3K	3.0
3K	SYN	2 – 28	2 – 115	3K – 5K	3.0
3L	SYN	2 – 28	2 – 115	5K – 7K	3.0
3M	SYN	2 – 28	2 – 115	7K – 10K	3.0
40	SYN	90	2 – 115	400 – 1K	3.0
41	RSL	90	2 – 115	400 – 1K	3.0
45	SYN	90	2 – 115	47 - 440	3.0
46	RSL	90	2 -- 115	47 - 440	3.0

Applicable Boards / Platforms

The following Boards / Platforms accept the 2nd generation D/S-R Modules shown above.

PLATFORM	P/N's
VME	**64CS4**
PCI	**76CS3**
3U cPCI	**75DS2**
6U cPCI	**78CS2**

Section III – Quick Start Guide

This section will provide the basic steps required to get a D/S-R up and running as quickly as possible. It covers the Analog interface connections and suggested software programming (Initialization) of a 2nd Generation D/S-R module.

Analog interface connections

Depending on the platform (75DS2, 76CS3, 78CS2 or 64CS4) and whether I/O interface is either Front or Rear, the connections available and proper connections will vary. Refer to Appendix B – Pin outs / I/O Signal definitions or to the Pin out information found in the Operations manual for the specific platform interface details.

Page one of Appendix B shows the full complement of possible signals available for the Analog interface.

(Note: not shown are two inputs, “TRIG1+” & “TRIG 1 -“. These are a differential pair to control the “Rotation Start” function in lieu of a digitally programmed Start command. Refer to the Operations Manual for pin out locations for this signal pair.)

The minimum critical signals required are;

- The Synchro or Resolver output Stator signals (S1 S2 S3 & S4) which must be connected to the load. S1, S2, S3 for a Synchro and S1, S2, S3 & S4 for a Resolver. For a Synchro, do not connect S4.

.

- If available at the I/O interface, the Sense lines **must be connected** in parallel with the above Stator signals. They may be connected remotely at the load or simply wrapped back at the I/O connector. I/O connector interfaces that do not provide the Sense lines have them connected internally on the modules.

- A proper Reference Voltage source must be connected to the RHI and RLO inputs. The source can be any Voltage from 2 to 115V rms and at a frequency consistent with the particular module being connected. e.g. for a two channel “2H” module, the reference frequency should be between 3 KHz and 5 KHz. This same reference typically must be supplied to the load device whether it’s a follow-up Servo system or a Solid State device such as an S/D or R/D converter.

  The reference source can be either an External signal, often supplied from the Unit Under Test (UUT) or from the Optional programmable reference supply offered with each Platform. The Optional reference source, if ordered, is not pre-wired to the Reference inputs. This programmable source is a stand alone, separate module on the card and its two wire output will be available on the I/O connector. The user must

refer to the Operations manual to locate the two pins carrying this source and they should be wired to the RHI & RLO inputs for each channel.

The balance of possible signals which may be available on the particular User I/O Analog Interface connector are for interfacing / controlling the NAI 44PA1 SBA. These signals and their application will be covered in a separate application note.

Initial Programming for start up

The following are the minimum programming suggestions for initializing each channel of D/S-R being utilized. It is suggested that the User's application software implement these functions on Start up instead of relying on Default values. Refer to the Operations Manual and the information provided in the Software Support Kit (SSK) provided for each Platform. Also, Appendix C shows the detail Register locations for each of these programmable functions. In the paragraphs below titles shown in Italics correspond to the register names in the Module Memory Map.

D/S Output Mode – The new converter designs provide the user with two options for setting the relationship between the Reference input voltage and the desired Output V L-L. Classically, D/S-R converters use a ***Ratiometric*** scheme whereby the factory programs a fixed "Turns ratio" between the Reference Input level and the Stator output signals (V L-L). Generally, this relationship is not field (user) programmable. For example a typical setup would be a user specified 26V reference input level with a requirement for an 11.8 V output. This represents a 0.454 TR. Thereafter, if the reference level varied up or down, the output level would vary by the same percentage. This mode can be selected and the TR is USER field programmable.

The 2nd generation converters offer a second mode of Reference Input level to Output level control referred to as ***Fixed*** mode. In this mode the user specifies a desired output signal level (V L-L) and the converter will hold that level regardless of Reference level input which can be any level from 2 to 115 V rms.

D/S Synchro / Resolver Select – While most of the available modules are either fixed as Synchro (S) or Resolver (R) outputs, it is suggested that this register be set to match the particular modules' specification. There are some modules which offer S or R programmability in which case the user can select the mode desired.

D/S Active Channel Select - To prevent false BIT (Built InTest) failure notices, this register should be set to show which channels are active. For each two channel or one channel module on a Platform, indicate as active only those channels which have a valid Reference applied and output enabled (*D/S Module Power Enable* as well as *D/S Output Enable* for one channel modules)

D/S Set Signal Volt Lo/Hi (CH 1/Ch 2) – Set these registers with the desired V L-L for each active channel. Selected voltage level must of course be within the range allowed for the particular module being used. This value will also be compared to the LOS (Loss Of Signal)Threshold level programmed to generate an LOS flag.

Signal Loss Threshold (CH 1/Ch 2) - Set these values for the Voltage level below which it is desired to generate a LOS flag. e.g. if the V L-L programmed to be supplied is 90 V, set the Threshold level at perhaps 80% or 72 V.

D/S Set Reference Volt Lo/Hi (CH 1/Ch 2) - Set these registers with the expected V level for the Reference being supplied. This is especially required if the ***Ratiometric*** output mode is selected in ***D/S Output Mode*** above. This value will also be compared to the LOR Threshold level programmed, to generate an LOR (Loss Of Reference) flag.

Reference Loss Threshold (CH 1/Ch 2) – Set these values for the Voltage level below which it is desired to generate a LOR flag. e.g. if the Reference to be supplied is 14 V, set the Threshold level at perhaps 80% or 11.2 V.

D/S Wrap Select, Internal/External – Normal operation without an external SBA requires that this register be set to "Internal" whereby the input to the Wrap S/D will be the Output of the D/S-R via the Sense lines. In the event the D/S-R output is driving an SBA and it is desired to monitor the Output of the SBA, then this register should be set to "External". For External selection, the BIT accuracy tolerance is adjusted to include the accuracy degradation due to the SBA.

D/S Set Phase offset – This register allows adjustment of the Phase Shift from the Reference to the Stator output signals. The Phase of the output signals compared to the reference signal is typically within 0.5 degrees. Actual CX devices have a leading phase shift in the order of 5 or 6 degrees and this is generally compensated for at the load device (either an S/D converter or a follow-up Servo). Therefore, to exactly duplicate a real CX, the user can program a phase shift to match the phase shift of the CX being simulated. In modern two speed systems the outputs (CX's) are supplied by Electrically wound two speed Resolvers and the multispeed channel NX can have fairly large phase shifts, in the order of 20 to 30 degrees. Again, precise simulation of these type outputs is possible using the Phase shift offset register. The range of offset is programmable from +90 to -90 degrees with a resolution of 0.1 degrees.

For driving Torque Receiver's, matching the D/S output phase shift to the receiver phase shift will significantly lower quiescent power.

D/S Module Power Enable & D/S Output enable – This step will turn on the D/S output amplifiers and present the required Stator signals to the Analog output connections.

For two channel modules, this register, "D/S Module Power Enable", will activate the output of both Channels by enabling the Converter Isolated Power Supplies. For one channel units in addition to "D/S Module Power Enable" the user must also program the register "D/S Output Enable" to complete the connection to the I/O interface. Allow a 2 second wait to allow the D/S Module outputs to Phase lock with the reference.

D/S Write Angle (Lo /Hi*)* – For each active channel, the D/S_R converters should be initialized to "0" degrees. In the event that the Platform RED bit LED is on, the user should clear the Status registers as described in "Section IV – BIT / Diagnostics / D3 detail setup". Follow Steps 5 & 6 for the "D3 BIT TEST PROCEDURE.

At this point the converters should be powered on and ready to accept programmed position angles. It is suggested that the user run a D3 BIT test as detailed in Section IV.

Section IV – BIT / Diagnostics / D3 detail setup

Summary

This section outlines the very powerful Diagnostic and BIT features of the 2nd generation D/S modules. Detail descriptions for D2 and D3 testing are shown below this summary. The significant features include;

- Continuous on line BIT for Accuracy via dedicated wrap S/D converters for each channel (D2 Test). (Test always active, status reporting can be disabled). D/S-R outputs are fed back to the Wrap S/D via the Sense lines. S/D digital output is continuously compared to the Commanded Angle and a difference of 0.2º will generate a "D/S Status BIT" error and will also energize the front panel RED BIT LED indicator.

- Offline D3 test. Similar to the D2 Test except the Commanded Angle is replaced by a test angle routine which generates 24 digital angles which are compared to the Wrap S/D output. Again, an accuracy difference of 0.2º will be flagged as a BIT error and energize the front panel RED BIT LED indicator.

- Separate Status Indicators are provided (written to registers) to pin point the source of a BIT error. All of these status errors may also result in a BIT error light since they may cause a D2 failure. If enabled, "Status Interrupts" will be flagged in the corresponding registers. Each "Status" can be individually enabled and Interrupt Vectors set in individual "Vector Interrupt" registers. These status indicators are;

  - D/S Status, BIT Test" – Indicates accuracy failure flagged by D2 / D3 Tests.

  - "Status Signal Loss" – Indicates that output VL-L has fallen below the value set by the user in the "Signal Loss Threshold" register.

  - "D/S Status, Reference Loss" – Indicates that the Reference Voltage input is below the value set by the user in the "Reference Loss Threshold" register.

  - "D/S Status, Phase Lock Loss" – Indicates that Phase lock has been lost between the Reference signal input and the D/S-R outputs

D/S BIT Test Enable

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X

Set bit to enable associated Built-In Self Test D2 or D3.

Detail D2 and D3 operation descriptions

The on-line (D2) Test - Writing "1" to the D2 bit of the BIT Test Enable Register initiates **status reporting** of the automatic background BIT testing. This testing continuously checks the output accuracy of each channel by comparing the measured output angle (via the Wrap S/D converter) to the commanded angle. The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from *D/S Status* registers within 2 seconds and if enabled, an interrupt will be generated. Writing a "0" deactivates the **status reporting**. The testing is totally transparent to the user, requires no external programming and has no effect on the standard operation of the module / card. Note: Outputs must be ON and a Reference supplied for test to function. Card will write 55h (every 0.1 seconds) to the *D/S Test (D2) Verify* register when D2 reporting is enabled. User can periodically clear to 00h and then read the *D/S Test (D2) Verify* register again, after 0.1 seconds, to verify that BIT Testing is activated. This test continuously monitors the measured angle and compares it to the Commanded "D/S Write Angle". If there is an error greater the 0.2º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.2º during a test cycle, the test cycle will not generally indicate an error.

The off-line (D3) Test - Writing "1" to the D3 bit of the BIT Test Enable Register initiates a BIT Test that generates and tests 24 different angles to an accuracy of 0.2°. External reference is required and outputs must be ON. The D/S Status bits will be set to indicate an accuracy problem. Results are available in the *D/S Test Status* registers and if enabled, an interrupt will be generated (See *Vector Interrupt* Registers). Test cycle takes about 30 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the *BIT Test Enable* register.

CAUTION: Outputs must be ON and Reference must be supplied during this test. The outputs are therefore active. Check connected loads for possible interaction.

D/S Status, BIT Test

Check the corresponding bit of the *D/S BIT Test Status* Register for status of BIT (Test-Accuracy) Testing for each "active" channel. A"1" means Accuracy Failed; "0" means Accuracy OK. Channels that are designated "inactive" are also set to "0" to preclude false BIT indications.. The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from D/S Status Registers within 2 seconds and, if enabled, an interrupt will be generated (See Interrupt Register).

D/S channels, by default, are set for monitoring the channel background BIT (Built-In-Test) status reporting; "ON" or "ACTIVE". The front panel BIT LED illuminates (Red) if any channel reports a BIT fault. For BIT status to work properly on an "active" channel, the D/S channel must have a valid Reference source applied and the D/S channel power set to "ON" (so there is a valid signal being generated). If channels are not being used, it is recommended that the channel BIT status report be turned off (or channel set INACTIVE). However, it should be noted that the channel BIT status register latches the contents of a failure until read. Simply setting the channel "INACTIVE" will not clear the BIT status register or extinguish the front panel BIT fault LED if a fault was previously detected.
The *D/S BIT Test Status* register should be queried (read) to insure the register is unlatched which will enable the BIT status register to be re-written during next status update (which, when the channel is set INACTIVE, should clear the fault). Once this is done, the front panel BIT LED will extinguish – as long as the channels that are active are working properly and the channels not being utilized are set INACTIVE.
Note: When *D/S Wrap Select External/Internal* register is set for "external", the BIT wrap will be read from the external amplifier wrap input signals (See pin-out). Also, the BIT tolerance will be adjusted for the amplifier accuracy specification.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, BIT Test	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Test (D2) Verify

Card will write 55h at Test (D2) Verify register when (D2)reporting is enabled, approximately every (1) second. User can clear to 00h and then read again, after approximately (1) second, to verify that background bit testing is activated.

D3 BIT TEST PROCEDURE: For PCI / cPCI (75DS2 / 76CS3 / 78CS2)

Below is a table which provides a detail step by step procedure for programming a (2) channel D/S module on a PCI / cPCI Platform and then running a D3 Test as a confidence check. The procedure and numbers suggested for Reference, Output Signal levels and for Threshold levels assume a module with programmable output range of 11.8 or 28 V L-L max.(all 1* & 3* modules). For 2* & 4* modules, (20 to 29 and 40 to 46) the voltage levels should be adjusted accordingly since these are 90 V L-L output modules. (Steps1-d through1-g). For 3* & 4* single channel modules, ignore references to Ch 2 in the procedure and note step **2-a** requirements.

Refer to Section II – (Applicable Modules and platforms) for details on 1*, 2*, 3* & 4* module characteristics.

D3 BIT TEST PROCEDURE: For VME platform 64CS4.

To run the D3 test for the VME Platform use the same procedure except all Hex Addr. Register values need to be divided by two. (See Appendix C memory maps).

Notes:

1. All registers Addresses mentioned below assume the module is in slot 1. Add base address offset of 0x800*(slotNum-1) when D/S module is in other slots.
2. Please access (read/write) in the order that is described below; otherwise, an undesired result might occur.
3. The value in Bit Status register is bit mapped per channel. Bit 0 for channel one and bit 1 for channel two. When the bit value is a logic 0, it means “NO BIT FAULT”. When the bit value is a logic 1, it means “BIT FAULT”.
4. D3 test result is only available at the end of the test. If one stops the test while it is running, the result is not guaranteed.

Step	***Description***	***Registers***
1.	**Connect a reference to the DS module for all channels (ch1, ch2,etc) from either an external / internal source. Assuming the ref voltage is 26Vrms and the module output is set to 11.8Vrms.**	
	1-a. Set all channels of DS to SYNCHRO MODE assuming the module hardware is a SYNCHRO.	**1-a)** Write 0xF to Addr(0x198)
	1-b. Set all channel of DS to RATIOMETRIC Output	**1-b** Write 0x0 to Addr(0x18C)

	1-c. Set all channel of DS to Active CHAN	**1-c)** Write 0x3 to Addr(0x1C8)
		1-d) Write 0xA28 to Addr(0x140) //Low Ch1
		1-d) Write 0x0 to Addr(0x144) //Hi Ch1
		1-d) Write 0xA28to Addr(0x148) //Low Ch2
		1-d) Write 0x0 to Addr(0x14C) //Hi Ch2

	1-d. Set exp ref voltage on the DS to 26V for Ch1 and Ch2.
	1-e Set exp line to line output on the DS to 11.8V for Ch1 and Ch2.
	1-f Set ref threshold voltage on the DS to 90% of exp ref for Ch1 and Ch2. 26*0.9=23.4V.
	1-g Set line to line threshold voltage on the DS to 90% of exp line to line output for Ch1 and Ch2.
	
	11.8*0.9=10.62V.
		1-e) Write 0x49C to Addr(0x160)//Low Ch1
		1-e) Write 0x0 to Addr(0x164)//Hi Ch1
		1-e) Write 0x49C to Addr(0x168)//Low Ch2
		1-e) Write 0x0 to Addr(0x16C)//Hi Ch2
		1-f) Write 0x924 to Addr(0x8C)//Ch1
		1-f) Write 0x924 to Addr(0x90)//Ch2
		1-g) Write 0x426 to Addr(0x80)//Ch1
		1-g) Write 0x426 to Addr(0x84)//Ch2

2.	Turn on DS module **2-a**. Output Enable (required for single chan. module) **2-b**. Module Power Enable (required for both single and dual channel modules).	**2-a)** Write 0x1 to Addr(0x1B0) **2-b)** Write 0x1 to Addr(0x1C0)
3.	Wait 2 seconds for DS module to phase lock with the reference	

4.	**4-a**.Initialize DS Ch1 output angle to 0 degrees.
	4-b.Initialize DS Ch1 output angle to 0 degrees.
	4-c.Initialize DS Ch2 output angle to 0 degrees.
	4-d.Initialize DS Ch2 output angle to 0 degrees.
		4-a) Write 0x0 to Addr(0xC0)//Lo Ch1
		4-b) Write 0x0 to Addr(0xC4)//Hi Ch1
		4-c) Write 0x0 to Addr(0xC8)//Lo Ch2
		4-d) Write 0x0 to Addr(0xCC)//Hi Ch2

5.	Make sure DS output is stable and all module statuses are good. The module statuses **are Bit, SigLoss, RefLoss, and PllLoss.** Make sure to have a few good successive statuses by reading all of the status registers. Put a delay of 500ms for each set of reading. All four registers should read 0x0 and that is considered as one successive status. A “0” in their respective registers is considered as a normal / (no fault) condition for all channels. The value of status registers are bit mapped to its channels. So, if the value	

	of the register showed a 0x3, that means chan1 and chan2 are currently faulted.
	5-a. Read signal loss status word for both chan1 and chan2 and ensure it is 0x0.
	5-b. Read ref loss status word for both chan1 and chan2 and ensure it is 0x0.
	5-c. Read bit loss status word for both chan1 and chan2 and ensure it is 0x0.
	5-d. Read phase loss status word for both chan1 and chan2 and ensure it is 0x0.
		5-a) Read Addr(0xB0) //signal loss status
		5-b) Read Addr(0x1CC) //ref loss status
		5-c) Read Addr(0x700) //bit loss status
		5-d) Read Addr(0x1D0) //phase loss status

6.	Read DS Bit Test Enable register (testEnb). Logically OR the content of DS Bit Test Enable register with 0x8(e.g. testEnb|=0x8); Write the value back to the DS Bit Test Enable register and this will trigger a D3 test to start. D/S steps its output angle every 15 degrees and stops when it reaches 345 degrees. It takes about 30 seconds to complete. At the end of the test, the value of DS Bit Test Enable register should be the same as pre-D3 test. You can also continuously read (poll) the DS Bit Test Enable register to determine whether D3 test has completed or not. Read the Bit status register for test result. Once again a "0" means normal(no faults) and other value (1,2 or 3) means a Bit failure on the respective channel. **6-a**. Read Bit Test Enable register **6-b**. Turn on D3 test by "OR'ing" 0x8 to the Bit Test Enable register. **6-c.** Write the "OR'ed" value to the Bit Test Enable register. **6-d**. Wait 30 seconds for D3 test to finish.	**6-a)** Read Addr(0x180) **6-b)** Logically "OR" the content of the address 0x180 with the value 0x8. **6-c)** Write the "OR"ed value to addr(0x180). **6-d)** Wait for 30 seconds

	6-e. The user can also monitor that the wrap angle is changing every 15 degrees. Read address 0x0 for chan1 wrap low word wrap angle. Read address 0x4 for chan1 wrap high word wrap angle. To get the actual angle, use this calculation: actualWrapAngle= ((wrapAngleHi<<16)+ (wrapAngleLow))*(360/2^32); **6-f.** Read Bit Test Enable register after D3 test has completed and its value should be same as pre-D3 test. **6-g**) Read Bit status registers to determine if D3 test had passed or failed.	**6-e)** Observe the wrap angle is reporting a 15 degrees increments for Ch1 and Ch2. Address 0x0 and 0x4 for Chan 1 wrap angle low word and ch1 wrap angle hi word respectively. **6-f)** After 30 seconds time has elapsed, read Addr (0x180) and its value should be the same as in step 6-a). **6-g)** Read addr (0x700) to determine if any bit fault had occurred.

Appendix A - Module detail Specifications.

The following detail specifications are shown here for the reader's convenience and as a reference only. Detail specifications are subject to change and changes will not be reflected in this document. The latest specifications are those shown in the "Operations Manuals" posted on our web site for each Platform.

D/S (Module 1*,2*) Two Isolated Digital-to-SYN/RSL Ch, 1.5/2.2 VA Outputs

***See P/N List –Section II**

(Applies to each channel unless noted otherwise)

Resolution:	16 bits (.0055°)
Accuracy:	±1 arc-minute (.017°) from No Load to Full Load
Output format:	Synchro or Resolver (see part number), galvanic isolation
Output voltage:	(See code table and part number).
Output load:	1.5 VA @ 11.8 VLL or 28 VLL, and 2.2 VA @ 90 VLL max. per Channel. Short circuit protected.
Output control:	Module outputs can be turned ON/OFF
Regulation (VL-L):	5% max. No load to Full load
Ratio:	Dual speed, Programmable, Set any ratio between 2 and 255
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.015°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS
Reference input voltage:	2 to 115 Vrms, Galvanic isolation. Requires 1 ma max/Channel
Reference frequency:	47 Hz to 10 kHz (See part number)
Phase shift:	0.5° max. (Between output and reference) (Programmable phase shift)
Settling time:	Less than 100 microseconds
Module Power:	+5VDC @ 570 mA ±12VDC @ 160 mA (no-load) per channel. (Add 2.9 watts of ±12VDC for every VA of output per channel). Therefore, a 1.5 VA Load adds to ±12V 181 mA average, or 288 mA peak per channel. External ±12V input power can be utilized. (PCI & cPCI Platforms)
Ground:	Isolated signal and reference. Channels individually isolated from each other and from system ground.

D/S (Modules 3*,4*) One Isolated Digital-to-SYN/RSL Ch, 3.0 VA output

***See P/N List –Section II**

(Will drive torque receivers. Applies to each channel unless noted otherwise)

Resolution:	16 bits (.0055°)
Accuracy:	0.067º (4 arc minutes) for passive loads; 30 arc minutes for TR's
Output format:	Synchro or Resolver, (see part number), galvanic isolation
Output voltage:	(See code table and part number).
Output load:	3.0 VA max./Channel. Short circuit protected.
Output control:	Channel output can be turned ON/OFF
Regulation (VL-L):	5% max. No load to Full load
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.15°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS
Reference input voltage:	2 to 115 Vrms, Galvanic isolation. Requires 1 ma max/Channel
Reference frequency:	47 Hz to 10 kHz (See part number)
Phase shift:	0.5° max. (Between output and reference) (Programmable phase shift)
Settling time:	Less than 100 microseconds
Module Power:	+5VDC @ 50 mA ±12VDC @ 115 mA (no-load); (Add 1.1 watts of ±12V for every VA of output). Therefore, a 3.0 VA Load adds to ±12VDC 138 mA average, or 157 mA peak). External ±12VDC input power can be utilized. (PCI & cPCI Platforms)
Ground:	Isolated signal and reference. Channels individually isolated from each other and from system ground.

Appendix B – Pin outs / I/O Signal definitions.

Note the following pin out tables are shown here for reference only and not a complete listing for each platform. For the complete pin out listings, please refer to the "Operations Manuals" posted on our web site for each Platform.

The 1 and 2 channel modules have different I/O signals available as shown below. However, due to pin out limitations (Front or Rear) on the various applicable platforms, the Sense lines and Synchro Booster Amplifier (44PA1) ON / Off, Analog feed back and BIT monitoring signals may not be available. Below is a table showing all the possible I/O connections for the one channel (3* & 4*) and two channel modules (1*& 2*)

I/O signals for 1 Channel & 2 Channel D/S-R modules

* Optional signals not always available at Board Front or Rear Connectors.

D/S[9] 1 Channel	D/S[9] 2 Channel	
	Ch1 S1	Min. required I/O connections to generate Synchro or Resolver output on Ch. 1
Ch1 S3	Ch1 S3	
Ch1 S1	Ch1 S2	
	Ch1 S4	
Ch1 RHI	Ch1 RHI	
Ch1 RLO	Ch1 RLO	
	Ch1 EXT-SIN-HI	* For interfacing with 44PA1 Synchro Booster Amplifier (SBA) feedback.
	Ch1 EXT-COS-HI	
	Ch1 EXT-GND	
	Ch2 S1	Min. required I/O connections to generate Synchro or Resolver output on Ch. 2
Ch1 S4	Ch2 S3	
Ch1 S2	Ch2 S2	
	Ch2 S4	
	Ch2 RHI	
	Ch2 RLO	
	Ch2 EXT-SIN-HI	* For interfacing with 44PA1 Synchro Booster Amplifier (SBA) feedback.
	Ch2 EXT-COS-HI	
	Ch2 EXT-GND	
	+5V	* For interfacing with 44PA1 Synchro Booster Amplifier (SBA) ON/OFF & BIT.
	Ch1 ON_OFF LO	
	+5V	
	Ch2 ON_OFF LO	
	Ch1 BIT HI	
	L/G (+5V return)	
	Ch2 BIT HI	
	L/G (+5V return)	
	Ch1 S1 SENSE	* Remote sense lines. If available, connect to S1, S2, S3, S4 at card interface or at load.
Ch1 S3 SENSE	Ch1 S3 SENSE	
Ch1 S1 SENSE	Ch1 S2 SENSE	
	Ch1 S4 SENSE	
	Ch2 S1 SENSE	
Ch1 S4 SENSE	Ch2 S3 SENSE	
Ch1 S2 SENSE	Ch2 S2 SENSE	
	Ch2 S4 SENSE	

spective
at output

Sense lines

Sense lines are provided for D/S output channels to compensate for voltage drops in the signal wiring. In applications utilizing the sense lines, wire the respective sense signal inputs in parallel with the signal output at the load if remote load sensing is required or at the output connector if remote load Sense is not required.

Front & Rear Pin outs for Various platforms .

PLATFORM	P/N's
VME	**64CS4**
PCI	**76CS3**
3U cPCI	**75DS2**
6U cPCI	**78CS2**

The following table shows the signals available for module slots 1 to 5 for the 64CS4 Platform. Slot 1 actual connector information is shown but it is representative of the available signals for Front and Rear connections for slots 2 through 5 as well. Note that using the Front I/O connector all signals available on the module are accessible. For rear I/O the SBA ON / OFF and Sense lines are not available. When not available, Sense lines are connected on the module at time of build.

SLOT 1 –1Ch, 2Ch D/S–R Typical Pin Outs (64CS4 Platform – 6uVME)

Front I/O	Rear I/O P2	D/S[9] 1 Channel	D/S[9] 2 Channel
J1-2	C18		Ch1 S1
J1-24	C22	Ch1 S3	Ch1 S3
J1-3	C20	Ch1 S1	Ch1 S2
J1-25	C24		Ch1 S4
J1-5	C29	Ch1 RHI	Ch1 RHI
J1-27	C27	Ch1 RLO	Ch1 RLO
J1-29	C14		Ch1 EXT-SIN-HI
J1-8	C12		Ch1 EXT-COS-HI
J1-7	C10		Ch1 EXT-GND
J1-12	C25		Ch2 S1
J1-34	C32	Ch1 S4	Ch2 S3
J1-13	C26	Ch1 S2	Ch2 S2
J1-35	C31		Ch2 S4
J1-15	A31		Ch2 RHI
J1-37	A32		Ch2 RLO
J1-39	A22		Ch2 EXT-SIN-HI
J1-18	A20		Ch2 EXT-COS-HI
J1-17	A18		Ch2 EXT-GND
J1-11	----		+5V
J1-33	----		Ch1 ON_OFF LO
J1-21	----		+5V
J1-43	----		Ch2 ON_OFF LO
J1-10	C28		Ch1 BIT HI
J1-32	C30		L/G
J1-20	A30		Ch2 BIT HI
J1-42	A29		L/G
J1-4			Ch1 S1 SENSE
J1-26		Ch1 S3 SENSE	Ch1 S3 SENSE
J1-6		Ch1 S1 SENSE	Ch1 S2 SENSE
J1-28			Ch1 S4 SENSE
J1-14			Ch2 S1 SENSE
J1-36		Ch1 S4 SENSE	Ch2 S3 SENSE
J1-16		Ch1 S2 SENSE	Ch2 S2 SENSE
J1-38			Ch2 S4 SENSE

For 64CS4, Slots 2 through 5, refer to the Operations manual for actual Front and rear connections.

Available module Pin Outs for the 76CS3, 75DS2 and 78CS2 Platforms.

76CS3 - (Full size PCI)

For the 76CS3, only front panel I/O is available. The table below shows the actual J1 Pin Outs for module slot 4 but is typical for slots 3 & 5 as well. (Refer to the 76CS3 Operations manual for actual pin outs for slots 3 & 5.)

As can be seen only the minimum connections to generate Synchro & Resolver outputs are available. Optional SBA control and Sense lines are not accessible on 76CS3.

SLOT 4 – 1Ch, 2Ch D/S–R Pin Outs (76CS3)

Front I/O J1		D/S 1 Channel	D/S 2 Channel
24			Ch1 S1
63		Ch1 S3	Ch1 S3
43		Ch1 S1	Ch1 S2
4			Ch1 S4
23		Ch1 RHI	Ch1 RHI
62		Ch1 RLO	Ch1 RLO
3			Ch2 S1
42		Ch1 S4	Ch2 S3
61		Ch1 S2	Ch2 S2
22			Ch2 S4
2			Ch2 RHI
41			Ch2 RLO

75DS2 (3u cPCI)

For the 75DS2 the following table shows the available signals available from the Front and Rear I/O connectors. Full signal functionality is available at the Rear (J2) connector. However the majority of the applications for the 75DS2 require PXI chassis compatibility which precludes the use of the rear I/O option. Shown in this Table are the slot 1 available functions. Slot 2 signals are identical except for actual Pin Out connections on J2 & J4. Refer to 75DS2 Operations Manual for Slot 2 pin outs.

SLOT 1 - 1Ch, 2Ch D/S–R Typical Pin Outs (75DS2)

Front I/O J4	Rear I/O J2	Slot 1 Single Channel D/S-R	Slot 1 Dual Channel D/S-R
1	E1		Ch.1-S1
2	E3	Ch1 S3	Ch.1-S3
3	E2	Ch1 S1	Ch.1-S2
4	E4		Ch.1-S4
5	D1	Ch1 RHI	Ch.1-RHi
30	D2	Ch1 RLO	Ch.1-RLo
26	C1		Ch.1- Sense S1
27	C3	Ch.1- Sense S3	Ch.1- Sense S3
28	C2	Ch.1- Sense S1	Ch.1- Sense S2
29	C4		Ch.1- Sense S4
6	E7		Ch.2-S1
7	E9	Ch1 S4	Ch.2-S3
8	E8	Ch1 S2	Ch.2-S2
9	E10		Ch.2-S4
10	D5		Ch.2-RHi
35	D6		Ch.2-RLo
31	C7		Ch.2- Sense S1
32	C9	Ch.1- Sense S4	Ch.2- Sense S3
33	C8	Ch.1- Sense S2	Ch.2- Sense S2
34	C10		Ch.2- Sense S4
21	D21	RHI-OUT	RHI-OUT
22	B21	+12V Ext	+12V Ext
23	F1	GND	GND
24	B19	-12V Ext	-12V Ext
25	---	TRIG1+	TRIG1+
---	B3		Ch1 EXT-SIN-HI
---	B2		Ch1 EXT-COS-HI
---	B1		Ch1 EXT-GND
---	B7		Ch2 EXT-SIN-HI
---	B6		Ch2 EXT-COS-HI
---	B5		Ch2 EXT-GND
---	A2		Ch 1 ON-OFF-HI (+5V)
---	A1		Ch1 ON-OFF-LO
---	A6		Ch 2 ON-OFF-HI (+5V)
---	A5		Ch2 ON-OFF-LO
---	A4		Ch1 BIT HI
---	A3		Ch1 BIT -LO (GND)
---	A8		Ch2 BIT HI
---	A7		Ch2 BIT -LO (GND)

Note: Remote Sensing is provided for each channel to eliminate errors caused by voltage drops on the interconnecting cables. The user must connect the load sense connections (i.e. Sense 1 - Sense S4) to the respective output signals. Connecting at the load is desirable to mitigate accuracy errors dependent on line and load resistance.

78CS2 (6u cPCI)

Below is the table showing the available Front and Rear I/O module signals. As can be seen, the available signals for Front & Rear connections are the same. However, the Sense lines are not available and are connected, at time of build, on the Module.

SBA On/Off, Feed back & BIT signals are available. The pin outs for slots 2 to 5 are the same except for the actual pins on the front and rear connectors. (Refer to the operations manual for actual slot pin outs for Slots 2 through 5)

SLOT 1 - 1Ch, 2Ch D/S–R Typical Pin Outs (78CS2)

Front I/O J7	Rear I/O J4	D/S 1 Channel	D/S 2 Channel
1	E25		Ch1 S1
21	E24	Ch1 S3	Ch1 S3
2	E23	Ch1 S1	Ch1 S2
22	E22		Ch1 S4
3	D25	Ch1 RHI	Ch1 RHI
23	D24	Ch1 RLO	Ch1 RLO
4	C25		Ch1 EXT-SIN-HI
24	C24		Ch1 EXT-COS-HI
5	C23		Ch1 EXT-GND
40	E19		Ch2 S1
60	E18	Ch1 S4	Ch2 S3
41	E17	Ch1 S2	Ch2 S2
61	E16		Ch2 S4
42	D19		Ch2 RHI
62	D18		Ch2 RLO
43	C19		Ch2 EXT-SIN-HI
63	C18		Ch2 EXT-COS-HI
44	C17		Ch2 EXT-GND
56	B5		+5V
76	B4		Ch1 ON_OFF LO
57	B3		+5V
77	B2		Ch2 ON_OFF LO
17	B11		Ch1 BIT HI
37	B10		L/G
18	B9		Ch2 BIT HI
38	B8		L/G

Appendix C – VME and PCI / cPCI Memory maps.

Note the following module Memory Maps tables are shown here for reference only. Additional features and hence registers may be added with time. and these tables will not necessarily reflect the updated lists. For the up to date memory Map listings, please refer to the "Operations Manuals" posted on our web site for each Platform.

D/S (1*, 2*, 3*, 4*) VME MODULE MEMORY MAP

000	Wrap S/D Angle Lo CH1	R	0A0	D/S Set Reference Volt Lo CH1	W/R	0F4	D/S Set Phase Offset CH1	W/R
002	Wrap S/D Angle Hi CH1	R	0A2	D/S Set Reference Volt Hi CH1	W/R	0F6	D/S Set Phase Offset CH2	W/R
004	Wrap S/D Angle Lo CH2	R	0A4	D/S Set Reference Volt Lo CH2	W/R	0FA	D/S Rotation Status CH1/2	R
006	Wrap S/D Angle Hi CH2	R	0A6	D/S Set Reference Volt Hi CH2	W/R			
						198	OSC Set Frequency Lo	W/R
032	Wrap S/D REF Voltage CH1	R	0B0	D/S Set Signal Volt Lo CH1	W/R	19A	OSC Set Frequency HI	W/R
034	Wrap S/D REF Voltage CH2	R	0B2	D/S Set Signal Volt Hi CH1	W/R	19C	OSC Set Voltage Lo	W/R
038	Wrap S/D Signal Voltage CH1	R	0B4	D/S Set Signal Volt Lo CH2	W/R	19E	OSC Set Voltage Hi	W/R
03A	Wrap S/D Signal Voltage CH2	R	0B6	D/S Set Signal Volt Hi CH2	W/R			
						1D0	D/S Start Rotation CH1	W
040	Wrap Signal Loss Threshold CH1	W/R	0BC	D/S Status, External Amplifier	R	1D2	D/S Start Rotation CH2	W
042	Wrap Signal Loss Threshold CH2	W/R	0BE	D/S Wrap Select, Internal/External	W/R	1D8	D/S Stop Rotation CH1	W
046	Wrap REF Loss Threshold CH1	W/R				1DA	D/S Stop Rotation CH2	W
048	Wrap REF Loss Threshold CH2	W/R	0C0	D/S BIT Test Enable	W/R			
			0C2	D/S Ratio 1/2	W/R	380	D/S Status, BIT Test	R
04C	Channel 1 Frequency	R	0C4	D2 Test Verify	W/R	382	D/S Reference Loss Interrupt Enable	W/R
04E	Channel 2 Frequency	R	0C6	D/S Output Mode	W/R	384	D/S Signal Loss Interrupt Enable	W/R
058	Status, Signal Loss	R	0C8	D/S Rotation Mode	W/R	386	D/S BIT FAIL Interrupt Enable	W/R
			0CC	D/S Synchro/Resolver Select	W/R	388	D/S Phase Lock Loss Interrupt Enable	W/R
060	D/S Write Angle Lo CH1	W/R	0CE	D/S Torque Receiver Select	W/R			
062	D/S Write Angle Hi CH1	W/R				3B4	Module Design Version	R
064	D/S Write Angle Lo CH2	W/R	0D0	D/S Trigger Source Select CH1	W/R	3B6	Module Design Revision	R
066	D/S Write Angle Hi CH2	W/R	0D2	D/S Trigger Source Select CH2	W/R	3B8	Module DSP Revision	R
072	D/S Stop Angle CH1	R	0D6	D/S Trigger Slope Select	W/R	3BA	Module FPGA Revision	R
074	D/S Stop Angle CH2	R	0D8	D/S Output Enable (1 CH only)	W/R	3BC	Module ID Revision	R
080	D/S Set Rotation Rate Lo CH1	W/R	0E0	D/S Module Power Enable	W/R	3E0	Vector Interrupt BIT Fail	W/R
082	D/S Set Rotation Rate Hi CH1	W/R	0E4	D/S Active Channel Select	W/R	3E2	Vector Interrupt Signal Loss	W/R
084	D/S Set Rotation Rate Lo CH2	W/R	0E6	D/S Reference Status	R	3E4	Vector Interrupt REF Loss	W/R
086	D/S Set Rotation Rate Hi CH2	W/R	0E8	D/S Phase Lock Status CH1/2	R	3E6	Vector Interrupt Phase Lock Loss	W/R

D/S (1*, 2*, 3*, 4*) PCI /cPCI MODULE MEMORY MAP

000	Wrap S/D Angle Lo CH1	R	140	D/S Set Reference Volt Lo CH1	W/R	1E8	D/S Set Phase Offset CH1	W/R
004	Wrap S/D Angle Hi CH1	R	144	D/S Set Reference Volt Hi CH1	W/R	1EC	D/S Set Phase Offset CH2	W/R
008	Wrap S/D Angle Lo CH2	R	148	D/S Set Reference Volt Lo CH2	W/R	1F4	D/S Rotation Status CH1/2	R
00C	Wrap S/D Angle Hi CH2	R	14C	D/S Set Reference Volt Hi CH2	W/R			
						330	OSC Set Frequency Lo	W/R
064	Measured Reference Voltage CH1	R	160	D/S Set Signal Volt Lo CH1	W/R	334	OSC Set Frequency HI	W/R
068	Measured Reference Voltage CH2	R	164	D/S Set Signal Volt Hi CH1	W/R	338	OSC Set Voltage Lo	W/R
070	Measured Signal Voltage CH1	R	168	D/S Set Signal Volt Lo CH2	W/R	33C	OSC Set Voltage Hi	W/R
074	Measured Signal Voltage CH2	R	16C	D/S Set Signal Volt Hi CH2	W/R			
						3A0	Start Rotation CH1	W
080	Signal Loss Threshold CH1	W/R	178	D/S Status, External Amplifier	R	3A4	Start Rotation CH2	W
084	Signal Loss Threshold CH2	W/R	17C	D/S Wrap Select, Internal/External	W/R	3B0	Stop Rotation CH1	W
08C	Reference Loss Threshold CH1	W/R				3B4	Stop Rotation CH2	W
090	Reference Loss Threshold CH2	W/R	180	D/S BIT Test Enable	W/R			
			184	D/S Ratio 1/2	W/R	700	D/S Status, BIT Test	R
098	Channel 1 Frequency	R	188	D2 Test Verify	W/R	704	Reference Loss Interrupt Enable	W/R
09C	Channel 2 Frequency	R	18C	D/S Output Mode	W/R	708	Signal Loss Interrupt Enable	W/R
0B0	Status, Signal Loss	R	190	D/S Rotation Mode	W/R	70C	BIT FAIL Interrupt Enable	W/R
			198	D/S Synchro/Resolver Select	W/R	710	Phase Lock Loss Interrupt Enable	W/R
0C0	D/S Write Angle Lo CH1	W/R	19C	D/S Torque Receiver Select	W/R			
0C4	D/S Write Angle Hi CH1	W/R				768	Module Design Version	R
0C8	D/S Write Angle Lo CH2	W/R	1A0	D/S Trigger Source Select CH1	W/R	76C	Module Design Revision	R
0CC	D/S Write Angle Hi CH2	W/R	1A4	D/S Trigger Source Select CH2	W/R	770	Module DSP Revision	R
0E4	D/S Stop Angle CH1	W/R	1AC	D/S Trigger Slope Select	W/R	774	Module FPGA Revision	R
0E8	D/S Stop Angle CH2	W/R	1B0	D/S Output Enable (1 CH only)	W/R	778	Module ID Revision	R
100	D/S Set Rotation Rate Lo CH1	W/R	1C0	D/S Module Power Enable	W/R	7C0	Vector Interrupt BIT Fail	W/R
104	D/S Set Rotation Rate Hi CH1	W/R	1C8	D/S Active Channel Select	W/R	7C4	Vector Interrupt Signal Loss	W/R
108	D/S Set Rotation Rate Lo CH2	W/R	1CC	D/S Status, Reference Loss	R	7C8	Vector Interrupt REF Loss	W/R
10C	D/S Set Rotation Rate Hi CH2	W/R	1D0	D/S Status, Phase Lock Loss CH1/2	R	7CC	Vector Interrupt Phase Lock Loss	W/R

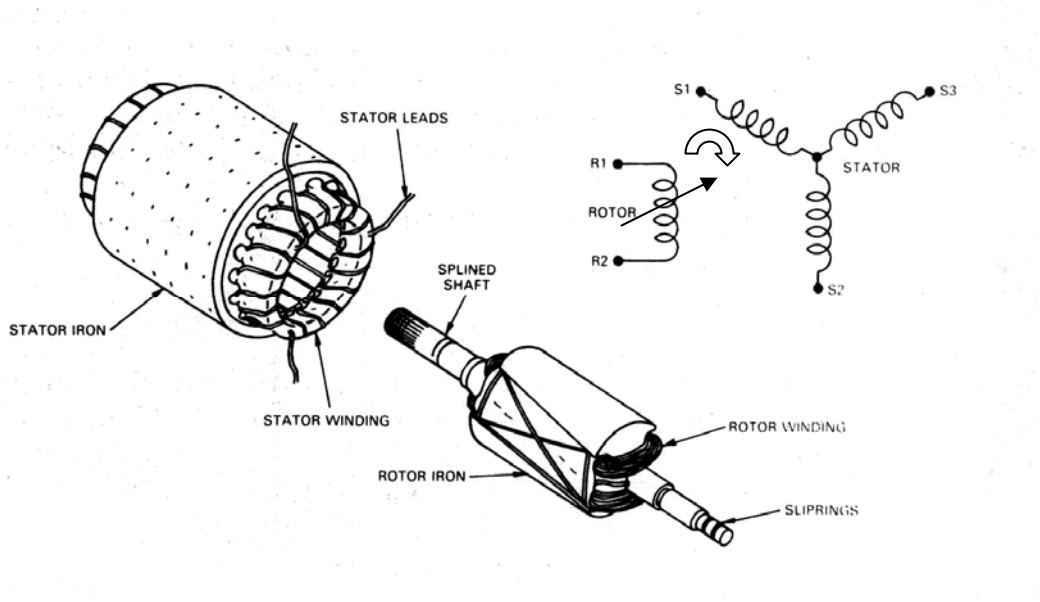
NOTE: The PCI / cPCI hex register locations are the same as VME locations x (2).
e.g. VME register 0x006 is same as PCI / cPCI register 0x00C.

Appendix D – Transducers, Synchros and Resolvers

Meet the Synchro CX (Synchro Transmitter)

The input is the R1 & R2 rotor excitation and the output are the three stator signals S1, S2 & S3. (A Synchro receiver, (CT) schematically, is the same except the inputs are the Stator signals from a CX)

The solid state equivalent of a CX / RX is a Digital / Synchro – Resolver converter, the focus of this application note.

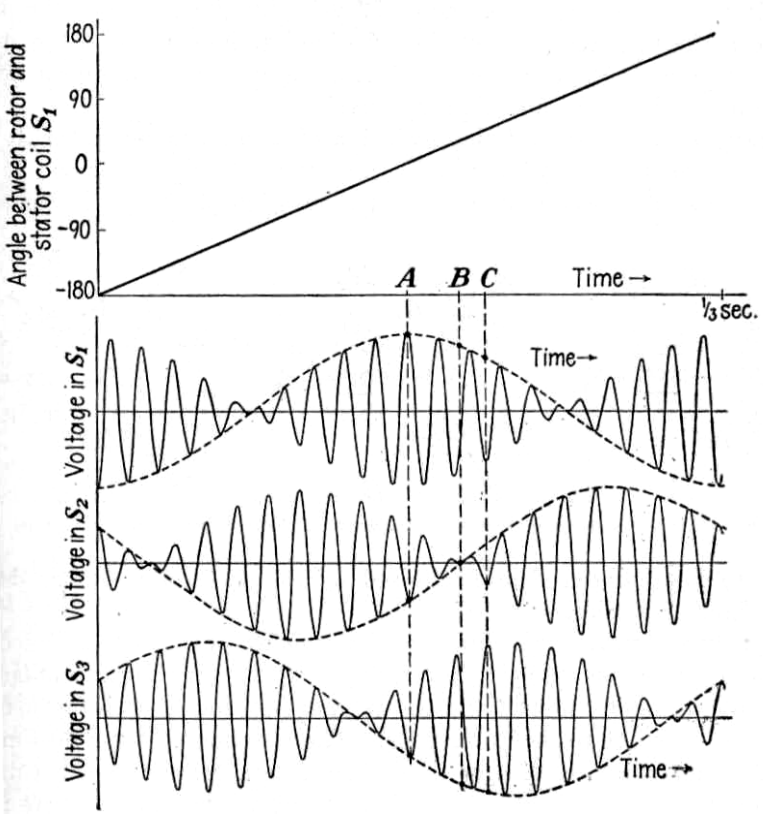


Synchro Voltages

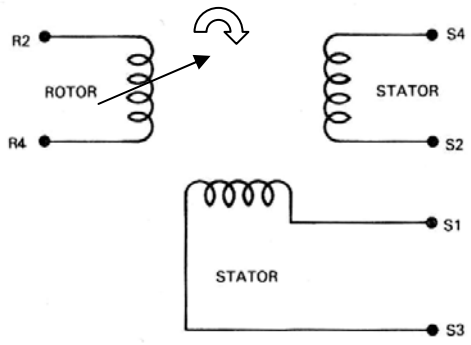
S1 to S3 = V_{ref} Sin 2πf . Sin θ
S3 to S2 = V_{ref} Sin 2πf. Sin (θ + 120^0)
S2 to S1 = V_{ref} Sin 2πf. Sin (θ + 240^0)
Where θ = shaft angle.
V_{ref} = reference voltage.
f = reference frequency

They look like small electric motors

Synchro voltages as shaft rotates



Meet the Resolver RX:



Resolver Voltages.

S1 to S3 = V_{ref} Sin 2πf.Sin θ
S4 to S2 = V_{ref} Sin 2πf.Cos θ
Where θ = shaft angle.
V_{ref} = reference voltage.
f = reference frequency.

While Synchro connections S1, S2 & S3 are well defined by MIL specs. (MIL-S-20708, MIL-STD-710, and MIL-HDBK-225A to name a few), Resolvers have no such standards and as such the S1, S2, S3 & S4 definitions are a free for all and vary among Resolver manufacturers as well as D/S-R converter manufacturers.

Naming conventions for Synchro and Resolver connections

Below are the NAI Standard naming conventions for Synchro and Resolver connections. Note, the X,Y, Z , R1, R2 symbols are the equivalent Synchro symbols from the old ARINC 407-1 Synchro specification for S1,S2, S3, RH, RL .

.

NAI Signals	Resolver	Synchro
S1	SIN(-)	X (S1)
S2	COS(+)	Z (S2)
S3	SIN(+)	Y (S3)
S4	COS(-)	No connect
RH	R1 or R3	R1 (RH)
RL	R2 or R4	R2 (RL)

NOTE:

- A resolver has the exact same function as a Synchro.
- Everything said about the Synchro is the same for a Resolver.
- The origin of the Synchro Resolver, to give its correct name, was to resolve angles into the Sine and Cosine components for gunnery computing, displays etc..
- Resolvers, especially electrically wound, multi-speed, have become increasingly popular and are being designed into many high speed applications in the military, industrial & automotive industries.

Basic Synchros and resolvers

There are two types of basic Synchros & Resolvers, Transmitters & Receivers

Transmitters (CX's / RX's) And Receivers (CT's / RT's).

Transmitter Synchros / Resolvers take a mechanical shaft input angle (θ = shaft angle) and a reference voltage, rotor input (V_{ref}) and generates stator output voltages which represent the equivalent electrical angle (ϕ) of the shaft input per the equations shown above for Synchro and Resolver output voltages.

A Receiver type Synchro / Resolver (CT / RT) takes in CX / RX generated stator voltages (ϕ) and generates an error signal on the rotor which represents the
Sine ($\theta - \phi$).

Digital to Synchro – Resolver (D/S-R) converters are simulation devices and are the solid state equivalents of CX's / RX's and the focus of this application note. It should be noted that all implementations of D/S converters are actually D/R converters and the output format (Synchro or Resolver) is determined in the output stage using a "Scott-T" circuit (transformers or solid state amplifiers) to go from Resolver format to Synchro format or just buffer amplifiers if Resolver signals are the desired output.

The Scott T transformer Function

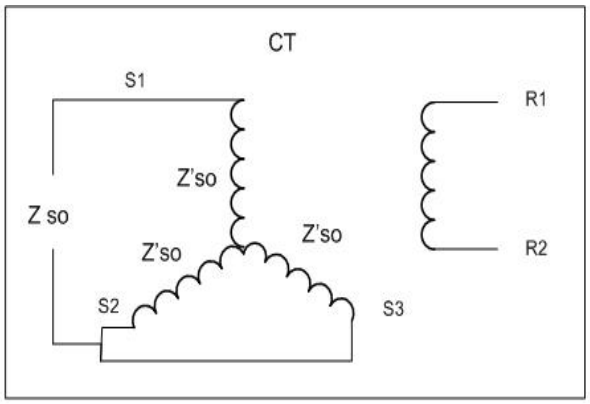
In modern D/S-R converters the Scott T function is implemented using power Op Amps and isolated DC to DC converters to maintain the same level of output isolation and accuracy achieved with actual transformers. Transformers are costly, bulky and a major source of error over frequency and load.

- This is a most important transformer connection that can change Synchro format 3 wire signals to resolver format 4 wire signals and vice versa.
- It allows all conversion and signal generation to be made using the Sine Cosine Resolver format that can be transformed to and from 3 wire Synchro format.
- A D/S is really a D/R with Scott T circuit on output.
- An S/D is really an R/D with Scott T at the input.
- The transformation operates in both directions

Loading

An important consideration in selecting a D/S-R converter is to make sure it has sufficient drive capability to drive the intended load. Drive capability is specified as VA (Volt Amperes) since actual CT's have Inductive impedance.

The key parameter needed for the Synchro or Resolver CT is Zso, For a 3 wire Synchro, Zso is the equivalent impedance with two of the Stator inputs tied together and measured to the third Stator lead. The Zso for a given CT or RT is specified by the manufacturer.



For resolver RT's, Zso is the impedance of one of the two input stator windings

To calculate the VA required for a Synchro CT load:
VA= ¾$(V_{L-L})^2$ / |Zso|

Where **V_{L-L}** is the D/S Line to Line output voltage

Where **|Zso|** is the absolute value of Zso

e.g. from the chart below and for a very common military CT (11CT4e
700 +j4900 and |Zso| is 4,950 **Ω**
Therefore required VA to drive an 11ct4e Synchro receiver is:

VA= ¾$(90)^2$ / 4950 = .75(8100) / 4950 = 1.23.
For Resolver RT loads, the calculation of VA is;

VA= $(V_{L-L})^2$ / |Zso|

For a typical 11.8V L-L, size 08, RT, |Zso| = 173Ω
VA = $(11.8)^2$ / 173 = 0.80

Tuning loads to reduce required VA

If the required VA is greater than available from the selected D/S, a technique is available to reduce the load VA. This is a method whereby the load can be "Tuned" using AC capacitors**.**

From the NAI Synchro Handbook Chapter 4, pages 32 & 33. (The entire handbook is available on the NAI website, under "Application Notes")

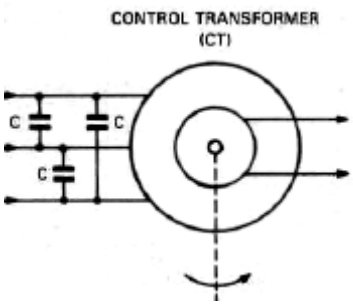


Figure 4.27 of Synchro Handbook CH 4

Note: As illustrated above, the Capacitors should be connected at the load in such a manner that the load cannot be separated from the capacitors. Other precautions are:

1.) The capacitors must be AC voltage rated.

2.) If the capacitors are not carefully matched, phase shifts will occur which will give rise to quadrature signals. The quadrature signals may be tolerable in many systems but could cause saturation of the servo system error amplifiers and asymmetrical limiting which may cause errors. The presence of quadrature will make phase shifts on the reference more critical.

(See section in Ch 4 of the Synchro Handbook on "Quadrature errors and reference phase shift".)

From the Hand Book, below are the formulas for calculating the proper value for the capacitors.

The values of the capacitors are given by:

$$C = \frac{Xso}{4\pi f\,(R^2 so + X^2 so)}$$

For example, in the case of an 11CT4C:

Zso = Rso +jXso = 700 + j4900

Therefore:

$$C = \frac{4900}{4 \times \pi \times 400(245 \times 10^5)} = 40 \text{ nf}$$

In the above 11CT4C example, untuned required power is;

$$(VA)_{untuned} = \frac{V^2{}_{L-L}}{|\,Zso\,|} \times \frac{3}{4} = \frac{90^2}{\sqrt{700^2 + 4900^2}} \times \frac{3}{4} = 1.23$$

Power required after tuning will be:

(VA) untuned x Rso / Zso

$$(VA)_{untuned} = 1.23 \times \frac{700}{4900} = 0.17 \text{ VA}$$

The tuning of Resolver loads is illustrated in figure 4.28 of Synchro Handbook CH 4 and the calculation is the same as for Synchros.

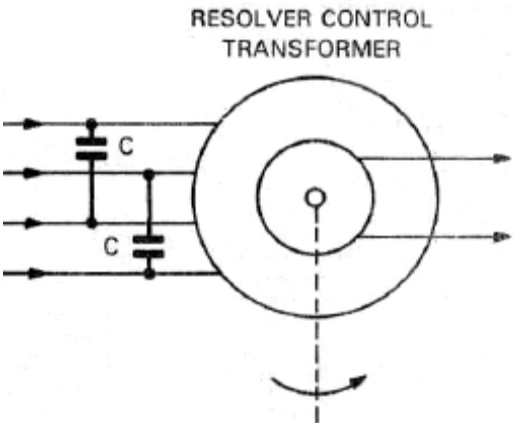


Figure 4.28 CH 4 Synchro Handbook

Zso / |Zso| values for Synchro & Resolver receivers

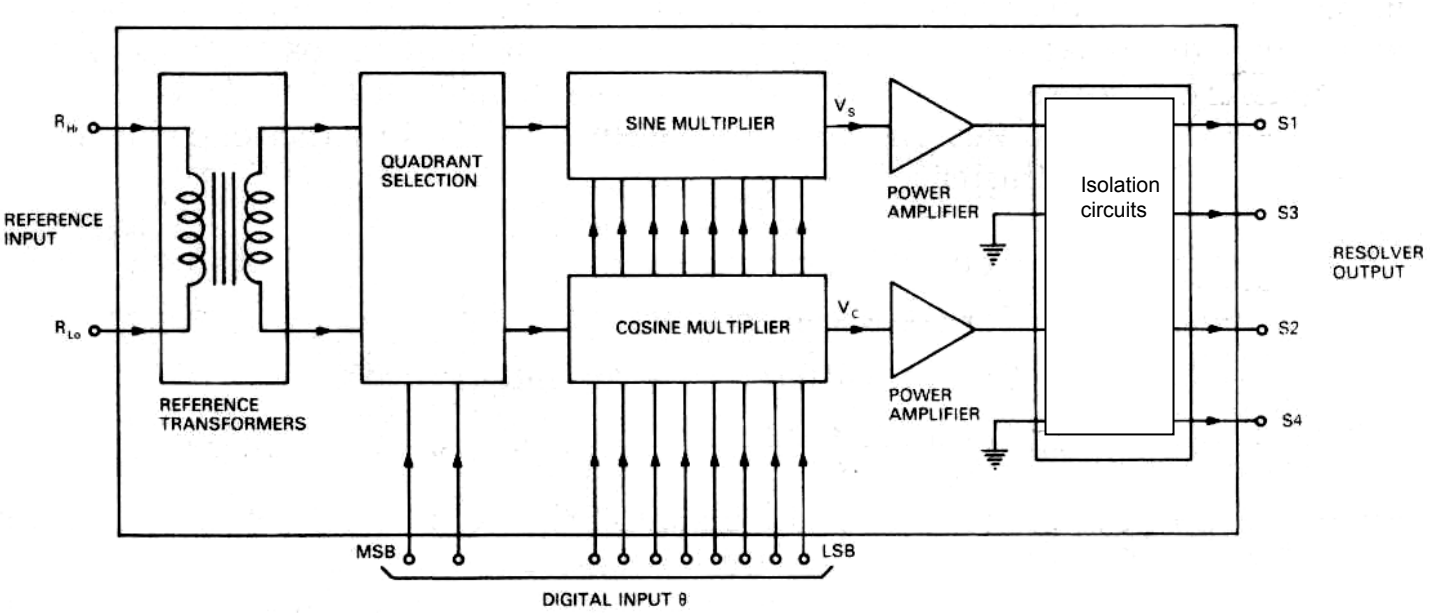
Some typical Zso and |Zso| values for Synchro CT's and Resolver RT's are shown below along with the calculated VA they require;

SOME TYPICAL MIL SYNCHRO CT's	FREQUENCY (Hz)	V_{L-L}	Z_{SO}	$\|Z_{SO}\|$ (OHMS)	VA
26V-08CT4B1	400	11.8	25+j93	96	1.09
26V-08CT4c	400	11.8	100+j506	516	0.202
26V-11CT4d	400	11.8	20+j128	130	0.8
11CT4e	400	90	700+j4900	4950	1.23
15CT4c	400	90	1020+j8330	8392	0.72
15CT6d	60	90	1140 + j6240	6343	0.96
18CT4c	400	90	1360 + 12600	12670	0.48
18CT6d	60	90	1690 + j4800	5089	1.19
23CT4c	400	90	1230 + 14300	14350	0.42
23CT6d	60	90	1380 + j4790	4985	1.22

SOME TYPICAL RESOLVER CT's	FREQUENCY (Hz)	V_{L-L}	Z_{SO}	$\|Z_{SO}\|$	VA
SIZE 08	400	5-26	250 + j790	828	0.82
SIZE 08	400	5-26	220 + j420	474	1.426
SIZE 08	400	11.8	45 + j168	173	0.8
SIZE 08	400	11.8	230 + j955	982	0.14
SIZE 11	400	0 -40	350 = j2220	2247	0.71
SIZE 11	400	0 -26	170 + j860	876	0.77
SIZE 11	400	5-40	620 + j2440	2517	0.63
SIZE 15	400	0 - 60	510 + j3200	3240	1.11
SIZE 15	400	0 - 60	300 + j1400	1431	2.51
SIZE 15	400	5-26	200 j1060	1078	0.63
SIZE 23	400	26	58 + j575	577	1.17
SIZE 23	400	0 - 90	360 + j2830	2852	2.8

Simplified basic D/S-R converter

Below is a very simplified D/R converter block Diagram. It shows that the reference input signal is applied to the equivalent of multiplying DAC's (Digital to Analog converters) which convert the Linear binary commanded angle into Digital Sine & Cosine inputs that then scale the input reference signal via the DAC's to the required Sine and Cosine signals. For a D/S converter the output isolation would be a Scott T Amplifier combination.



Appendix E – Glossary of terms and abbreviations

BIT	Built In Test
BW	Band Width
cPCI	compactPCI- an electrical superset of PCI for desktops and also with different form factors
CT	Synchro Control Transformer (Receiver)
CX	Synchro Control Transmitter
D / S-R	Digital to Synchro or Resolver Converter, also D/S or D/R
DAC	Digital to Analog Converter. Also D/A
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
LOR	Loss of Reference
LOS	Loss of Signal
NAI	North Atlantic Industries
PCI	Peripheral Component Interconnect - a computer parallel electrical BUS & size standard for attaching hardware devices to the Processor. Usually in a Desktop computer
R	Resolver
RT	Resolver Control Transformer (Receiver)
RX	Resolver Control Transmitter
S	Synchro
SBA	Synchro Booster Amplifier
S-R / D	Synchro or Resolver to Digital Converter, also S/D or R/D
SSK	Software Support Kit
TR	Torque Receiver type Synchro, also Turns Ratio.
TX	Torque Transmitter type Synchro.
UUT	Unit Under Test
V L-L	Line to Line V (rms) - Stator inputs or outputs for Synchros and Resolvers
V REF	Voltage level (rms) of Synchro or Resolver Reference inputs. Also reference input to D/S-R
VA	Volt-Amperes - measure of Reactive (imaginary) power required for an inductive or capacitive load
VME	Virtual Module Eurocard - a computer parallel BUS & physical size standard.
WSD	Wrap S/D Converter
Zso	Equivalent reactive impedance of a 3 wire Synchro Stator set or 2 wire reactive impedence of either the Sine or Cosine stator winding of a Resolver. Zso is expressed as R+jR.
|Zso|	Magnitude of resultant vector of Zso. The square root of $R^2 + jR^2$

Revision Page

Revision	Description of Change	Engineer	Date
Rev 1	Preliminary Release.	FR	12/05/2010
Rev 2	Renamed from AN002 to AN006. Incorporated suggestions.	FR	12/13/2010
Rev 3	Initial release. Reorganized sections and appendices for ease of use. Corrected / enhanced Appendix D	FR	01/05/2011